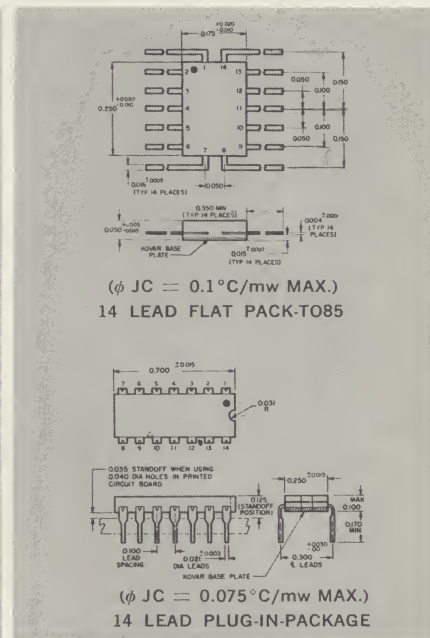
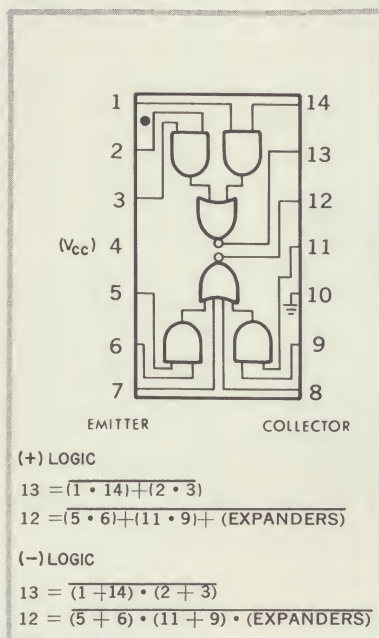
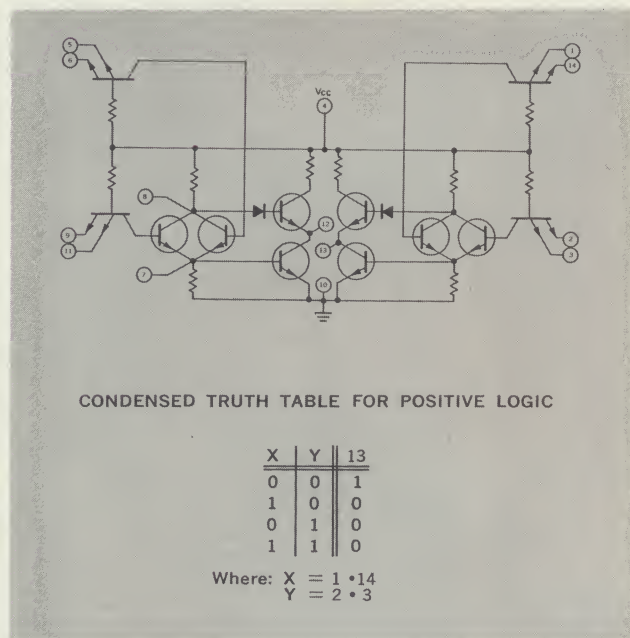


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**Expandable Dual Output,
Dual 2-Input AND-NOR Gate
SG70/SG71**

Monolithic Silicon Epitaxial Circuit For Military Temp. Range -55°C to +125°C



CIRCUIT DESCRIPTION:

The **SG70** and **SG71** gates are members of the SUHL* family of logic elements which is a monolithic, epitaxial, saturated high speed logic family. Each package contains two circuits. Each circuit consists of two 2-input AND gates which are OR'ed together and then inverted. The OR points of one circuit are brought out to permit further expansion of the OR function by means of the SG150 and the SG170 series expanders. The gate functions as an AND-NOR element in positive logic for exclusive-OR, "wired-OR" and comparative functions. The circuit is designed for high speed operation over the military temperature range of -55°C to +125°C without sacrificing characteristics of fan out, logic swing, noise immunity and capacitance drive at low power.

This circuit requires a single power supply and has the following outstanding features:

CHARACTERISTICS SUMMARY:

1. High fan out: 15 min for **SG70**; 7 min for **SG71**.
2. High speed: Designed to operate at 20 mc, propagation delay time is typically 12 nsec.
3. High Noise immunity: ± 900 mV at 25°C and worst case fan out; ± 450 mV from -55°C to +125°C at worst case fan out; ± 600 mV from 0°C to +75°C at worst case fan out.
4. High capacitance drive: Up to 600 pf.
5. High logic swing: Logic 0 is typically 0.26 volts; Logic 1 is typically 3.3 volts at 25°C.
6. Short circuit protection.
7. Low power: 20 mw average dissipation.
8. Low output impedance in the "0" and "1" level reduces noise pickup.
9. No complex loading rules since input and output are isolated.
10. Expandable OR: By using SG150 and SG170 series OR expanders, "wired OR" of up to 10 gates can be obtained.

These features offer to the logic designer for the first time in an integrated circuit the combined advantage of speed at low power, high reliability and a high degree of logic flexibility. The result is a digital element that facilitates system design when combined with other SUHL elements.

* Sylvania Universal High Level Logic

RATINGS

Min. Typical Max.

Min. Typical Max.

VOLTAGE			TEMPERATURE AND POWER		
Supply voltage (D.C.)		8.0 V	Operating	-55	+125°C
Supply voltage (surge, 1 sec)		12.0 V	Storage	-65	+200°C
Supply voltage (operating)	4.5	5.0	Thermal gradient, junction to air (θ_{ja}) (FLAT PACK)		0.3°C/MW
Input voltage		5.5 V	Thermal gradient, junction to air (θ_{ja}) (PLUG-IN)		0.15°C/MW
Output voltage		5.5 V	Power Dissipation (50% Duty Cycle, $V_{cc} = +5V$)	20	MW/Circuit

ELECTRICAL SPECIFICATIONS

		Values at Specified Temperatures				
Characteristics at $V_{cc} = +5.0V$		Symbol	-55°C	+25°C	+125°C	Units
INPUT:						
Input Load Current @ $V_{IN} =$	I_{IN}	1.33	1.33	1.33	mA Max.	1
Other Inputs		0	0	0	Volts	
Input Leakage Current @ $V_{IN} =$	I_{IN}	0.1	0.1	0.1	mA Max.	2
Other Inputs		4.5	4.5	4.5	Volts	
Inverse Beta Current @ $V_{IN} =$	I_{IN}	0.1	0.1	0.1	mA Max.	3
Other Inputs		4.5	4.5	4.5	Volts	
Input (OFF Level) Breakdown Voltage $I_{IN} =$	$BV_{IN} "1"$	5.5	5.5	5.5	Volts	2
Other Inputs		1.0	1.0	1.0	mA Max.	
Input (ON Level) Breakdown Voltage $I_{IN} =$	$BV_{IN} "0"$	5.5	5.5	5.5	Volts	3
Other Inputs		1.0	1.0	1.0	mA Max.	
Logic "1" Threshold Voltage $V_{OUT} =$	$V_{MIN} "1"$	2.0	1.7	1.4	Volts	8
$I_{OUT} (SG70)$		0.45	0.45	0.45	Volts Max.	
$I_{OUT} (SG71)$		20	20	20	mA	
Logic "0" Threshold Voltage $V_{OUT} =$	$V_{MAX} "0"$	1.0	1.2	0.9	Volts	9
$I_{OUT} (SG70)$		2.5	2.4	2.7	Volts Min.	
$I_{OUT} (SG71)$		1.5	1.5	1.5	mA	
OUTPUT:						
Output Leakage Current @ $V_{OUT} =$	I_{OUT}	0.25	0.25	0.25	mA Max.	5
Inputs		5.5	5.5	5.5	Volts	
Output Short Circuit Current @ Input	I_{OUT}	10	10	10	mA Min.	7
Logic "0" Level @ $V_{IN} =$	$V_{OUT} "0"$	0.40	0.40	0.45	Volts Max.	
$I_{OUT} (SG70)$		2.8	2.8	2.8	Volts	8
$I_{OUT} (SG71)$		20	20	20	mA	
Logic "1" Level @ $V_{IN} =$	$V_{OUT} "1"$	2.8	3.2	3.35	Volts Min.	9
$I_{OUT} (SG70)$		0.45	0.45	0.45	Volts	
$I_{OUT} (SG71)$		1.5	1.5	1.5	mA	
POWER REQUIREMENTS:						
Breakdown Current @ $V =$	I_{CC}	10	8		mA Max.	4
Inputs		0	0		Volts	
"ON" State Current Drain Inputs	$I_{CC} "0"$	14	14	14	mA Max.	6
"OFF" State Current Drain Inputs	$I_{CC} "1"$	Open	Open	Open	Volts	
		7.0	7.0	7.0	mA Max.	4
		0	0	0	Volts	

TYPICAL TEST CONFIGURATION

Fig. No. 1

Fig. No. 2

Fig. No. 3

Fig. No. 4

Fig. No. 5

Fig. No. 6

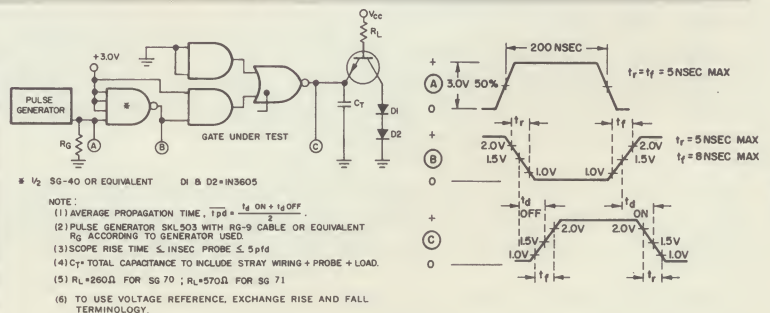
Fig. No. 7

Fig. No. 8

Fig. No. 9

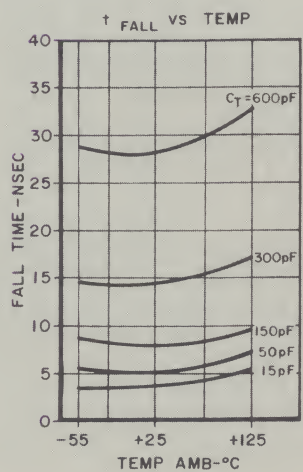
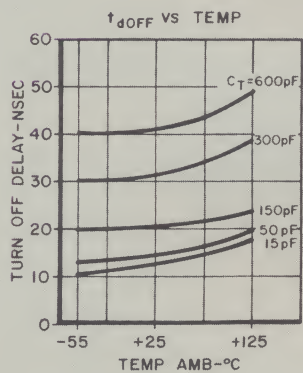
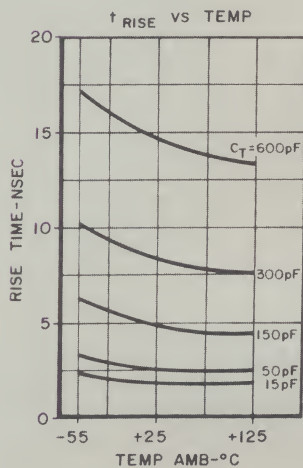
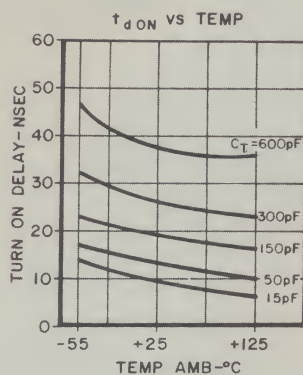
SWITCHING SPECIFICATIONS

SWITCHING PARAMETERS	CONDITIONS		LIMITS	
	V_{cc} volts	T_A °C	FANOUT	TIME — nsec
			SG70	SG71
Turn On Delay	+5.0	+25	15	7
Turn Off Delay			15	7
Rise Time Note 6			15	7
Fall Time Note 6			15	7

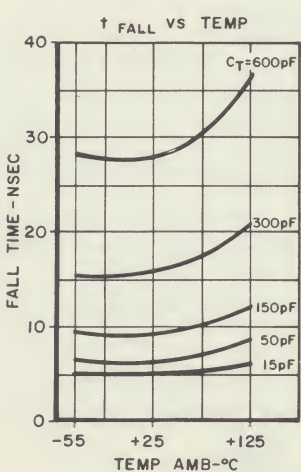
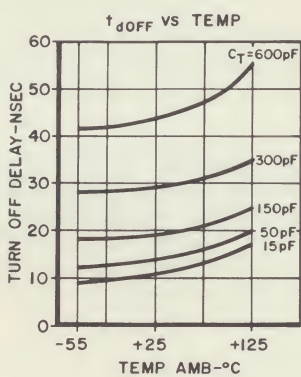
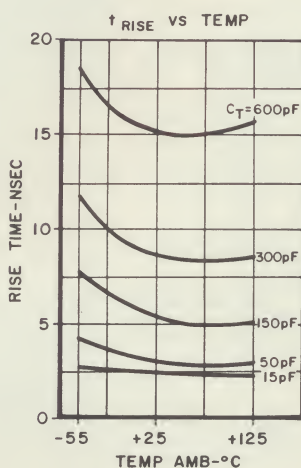
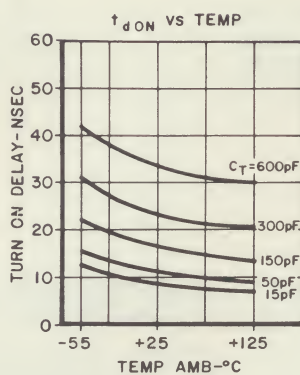


TYPICAL SWITCHING CHARACTERISTICS: $V_{CC} = +5.0V$

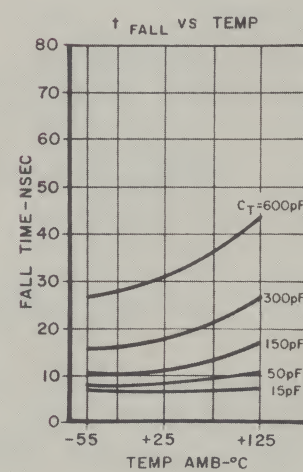
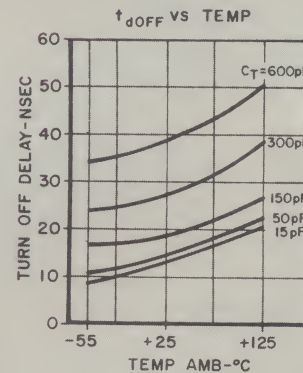
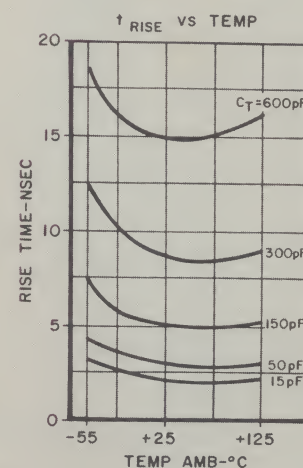
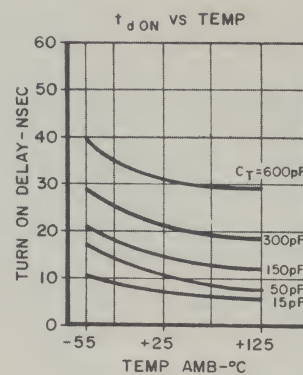
FAN OUT = 1



FAN OUT = 7



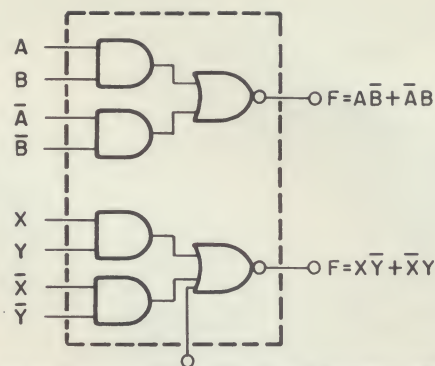
FAN OUT = 15



APPLICATION 1.

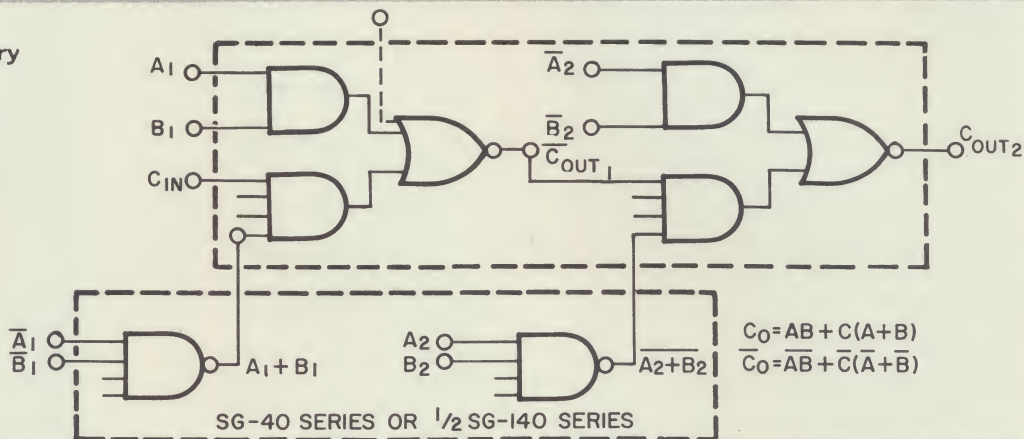
Exclusive OR

This circuit performs the dual Exclusive OR function in one package where the input functions and their complement are available. The propagation delay is the delay of one stage.



APPLICATION 2.

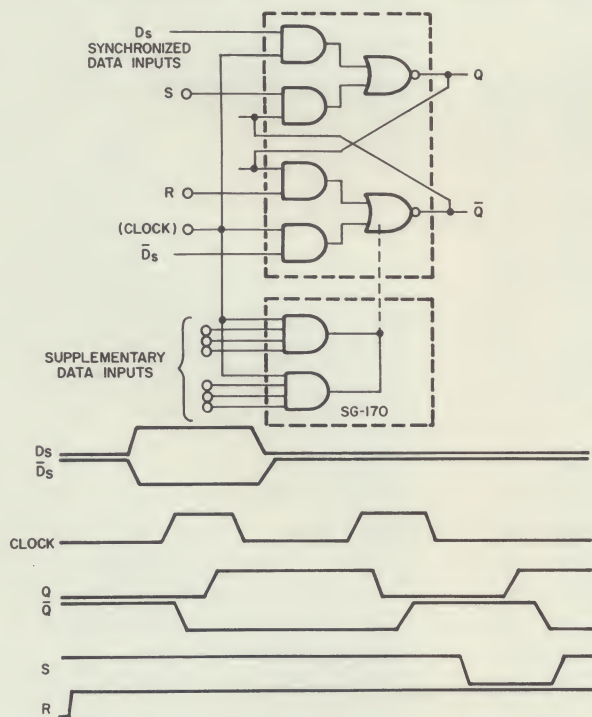
Half-Adder — Single Stage Carry



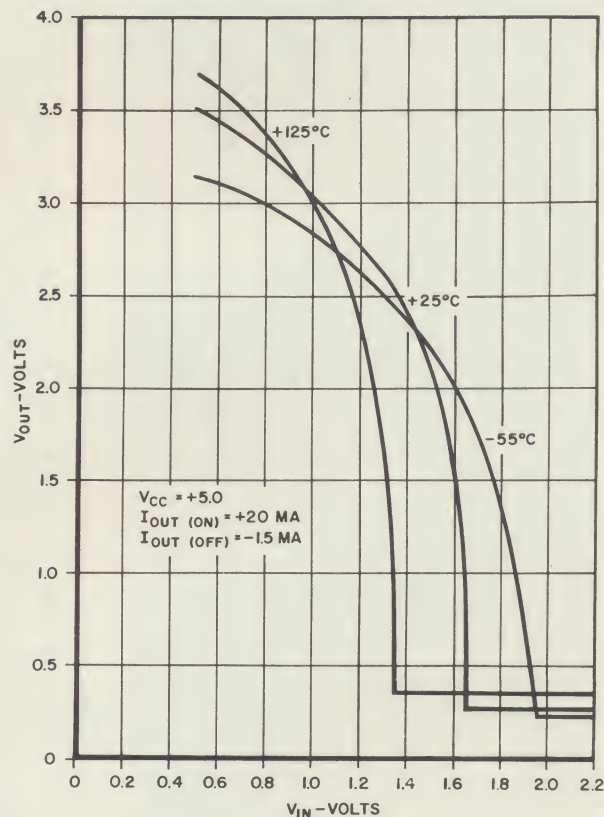
APPLICATION 3.

Half Shift Register

HALF SHIFT REGISTER WITH SUPPLEMENTARY DATA INPUTS



TYPICAL V_{IN} - V_{OUT} TRANSFER CHARACTERISTIC -55°C TO +125°C



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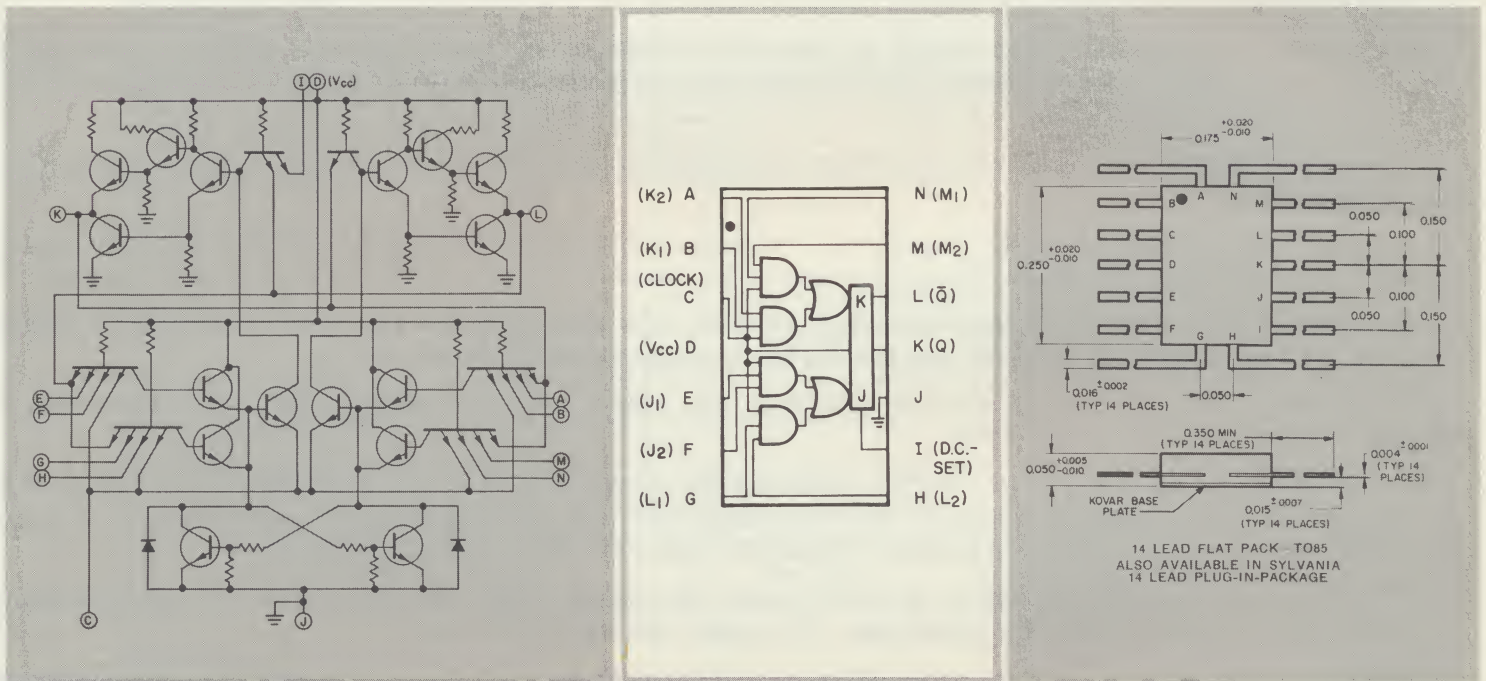
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10/1/66

OR Input J-K Flip-Flop
SF60/SF61

Monolithic Silicon Epitaxial Circuit For Military Temp. Range -55°C to +125°C



CIRCUIT DESCRIPTION

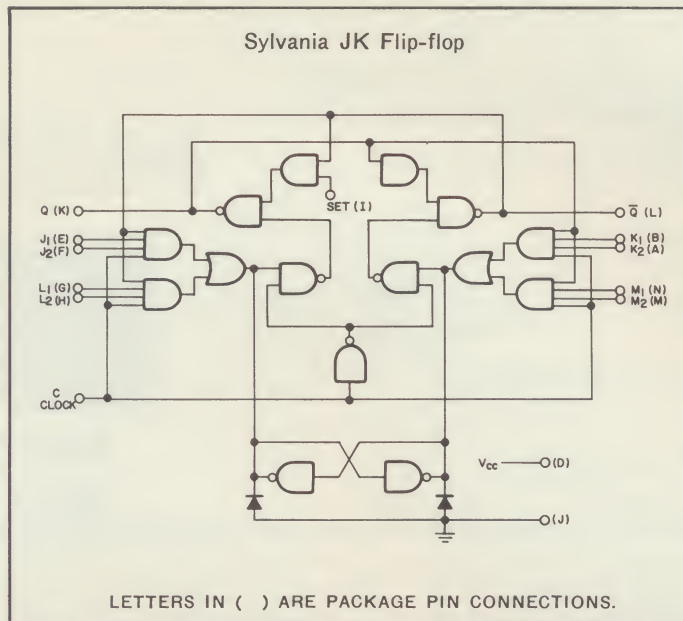
The **SF-60** and **SF-61** are J-K flip-flops with ORed data inputs. They are members of the SUHL* family, which is a monolithic epitaxial, saturated high speed type of logic. The circuit is designed with the system requirements in mind permitting high speed systems with a saving on gates and interconnections. The SF-60 and SF-61 operate up to 20 megacycles over the temperature range of -55°C to $+125^{\circ}\text{C}$ for military ground support and industrial systems while maintaining SUHL* characteristics of fan-out, logic swing, noise immunity and capacitance drive at low power. The SUHL* J-K flip-flop operates from a single 5.0 V power supply.

Data can be fed into the J, L, K and M inputs (two of each) while the clock is low. The J and L inputs are ORed; the K and M inputs are ORed. The results of the ORing is ANDed with the clock and the present state of the flip-flop (the state of the flip-flop is fed back to the input terminals via the connection from the Q and $\bar{Q}$ terminals to the K, M and J, L terminals respectively) and stored in the depletion region of a diode when the clock goes high. When the clock returns low the stored information is ANDed with the inverted clock, causing the cross coupled NAND gates to be set accordingly.

*Sylvania Universal High level Logic

CHARACTERISTIC SUMMARY

1) Logic at the inputs—In addition to the basic J-K flip-flop function of determinate output states for every input condition, the Sylvania **SF-60** and **SF-61** have two J, two L and two K, two M data inputs which can be used to provide the AND-OR function right in the flip-flop. This provides greater system speed equivalent to the speed of the flip-flop and reduces the number of external gates necessary to perform system operations.**



LOGIC EQUATIONS

$$Q_{n+1} = (J+L) \bar{Q}_n + (K+M) Q_n$$

where
 $J = J_1 \cdot J_2$ and $L = L_1 \cdot L_2$
 $K = K_1 \cdot K_2$ and $M = M_1 \cdot M_2$

$$Q_{n+1} = (J+L) \bar{Q}_n + (K+M) Q_n$$

SEQUENTIAL STATES

Q _n	Q _{n+1}	J	L	K	M
0	0	0	0	Ø	Ø
0	1	1	Ø	Ø	Ø
0	1	Ø	1	Ø	Ø
1	1	Ø	Ø	0	0
1	0	Ø	Ø	1	1
1	0	Ø	Ø	Ø	1

Ø = Don't Care

TRUTH TABLES

- 2) Internal Complementing—The circuits are internally complemented which means all inputs are usable as data inputs in all systems. This provides maximum speed and maximum fan-out from the flip-flop itself and simplifies systems wiring.
- 3) Operation at low frequencies and clock edges as long as 200 nanosecs is made possible by use of charge control devices.
- 4) Operation at frequencies greater than 20 mc is made possible by using charge control devices (instead of a master slave operation) coupled with a discharge network which removes any excess stored charge at high frequency.
- 5) Negative edge triggering—Triggering is done when the clock goes negative. This permits the rest of the system to be inhibited (positive logic) at the time the flip-flop is going through its translation.
- 6) Raceless—The inhibiting action of the clock input also directly inhibits the data terminals thus preventing any race problem internal to the flip-flop.
- 7) Raceless in a system where one flip-flop drives another. Data should be present when the clock goes high. If the data changes while the clock is high the flip-flop requires 300 nsec to recognize a change from 1 to 0; 10 nsec to recognize a change from 0 to 1. In addition the delay through a flip-flop is greater than 8 nsec.
- 8) Triggers on clock pulses as narrow as 20 nanosecs;† the charge storage (memory of data on input terminals) is accomplished rapidly through low impedances. No master flip-flop has to be set.
- 9) Noise immune clock—Triggers on the voltage level of the clock and can therefore tolerate high noise on the clock when it is in the "1" or the "0" position. Because of this characteristic the clock input is also tolerant to overshoot up to the positive breakdown voltage and to 0.5 V below ground.
- 10) Provides asynchronous (direct) SET terminal which represents a gate load of 1 and is independent of the clock. The application of a "0" will cause Q to go to "1".
- 11) All data terminals represent a gate loading of one. The clock terminal represents a gate loading of 3.0.
- 12) High fan-out: 15 min. for **SF-60**; 7 min. for **SF-61**.
- 13) High speed: 20 mc clock. Propagation delay times typically
13 nsec t_{off} , 25 nsec t_{on}
- 14) High noise immunity ± 900 mv at 25°C and worse case fan-out
 ± 450 mv from -55°C to +125°C and worse case fan-out.
- 15) High capacitance drive up to 600 pf.
- 16) High logic swing: Logic 0 is typically 0.26 volts, Logic 1 is typically 3.3 volts at 25°C.
- 17) Low power: typically 60 milliwatts.
- 18) Low output impedance in the "0" and "1" level reduces noise pick-up.

†Unused emitters tied to 2.0 to 5.5 V; or unused data inputs tied to the clock, set terminal tied to $\bar{Q}$

**See applications on back page

RATINGS

Min. Typical Max.

Min. Typical Max.

VOLTAGE

Supply voltage (D.C.)			8.0 V
Supply voltage (surge, 1 sec)			12.0 V
Supply voltage (operating)	4.5	5.0	6.0 V
Input voltage			5.5 V
Output voltage			5.5 V

TEMPERATURE and POWER

Operating	-55		+125°C
Storage	-65		+200°C
Thermal gradient, junction to air (θ_{ja})			0.3°C/MW
Thermal gradient, junction to case (θ_{jc})			0.1°C/MW
Power Dissipation (50% Duty Cycle, $V_{CC} = +5V$)		60	MW

ELECTRICAL CHARACTERISTICS

Characteristics at $V_{CC} = +5.0V$	Symbol	Values at Required Temperatures			Units
		-55°C	+25°C	+125°C	
INPUT:					
Input Load Current (For set) @ V_{IN} and Clock Other Inputs: Q Low when checking Set	I_L	1.33 0 +4.5	1.33 0 +4.5	1.33 0 +4.5	mA Max. Volts Volts
Input Load Current (For $J_1, J_2, L_1, L_2, K_1, K_2, M_1, M_2$) @ $V_{IN} =$ Other Inputs: Q Low when checking J_1, J_2, L_1, L_2 Set Low when checking K_1, K_2, M_1, M_2	I_L	1.33 0 +4.5	1.33 0 +4.5	1.33 0 +4.5	mA Max. Volts Volts
Input Load Current (for Clock) @ $V_{IN} =$ Others	I_L	4.0 0 +4.5	4.0 0 +4.5	4.0 0 +4.5	mA Max. Volts Volts
Input Leakage Current (All except Clock) @ $V_{IN} =$ Other Inputs: $\bar{Q}$ Low when checking Set, J_1, J_2, L_1, L_2 Q Low when checking K_1, K_2, M_1, M_2 (Set Open)	I_{INLK}	0.1 +4.5 0	0.1 +4.5 0	0.1 +4.5 0	mA Max. Volts Volts
Input Leakage Current (for Clock) @ $V_{IN} =$ Other Inputs (Set Open)	I_{INLK}	0.3 +4.5 0	0.3 +4.5 0	0.3 +4.5 0	mA Max. Volts Volts
Inverse Beta Current (All except Clock) @ $V_{IN} =$ Other Inputs: Q Low when checking Set, J_1, J_2, L_1, L_2 Set Low when checking K_1, K_2, M_1, M_2	$I_{B_{INV}}$	0.1 +4.5 Open	0.1 +4.5 Open	0.1 +4.5 Open	mA Max. Volts Volts
Inverse Beta Current (Clock) @ $V_{IN} =$ Other Inputs: Q Low when checking Clock Input at J Side Set Low when checking Clock K Side	$I_{B_{INV}}$	1.6 +4.5 Open	1.6 +4.5 Open	1.6 +4.5 Open	mA Max. Volts Volts
Input (OFF Level) Breakdown Voltage ($J_1, J_2, L_1, L_2, K_1, K_2, M_1, M_2$) @ $I_{IN} =$ Other Inputs: $\bar{Q}$ Low when checking Set, J_1, J_2, L_1, L_2 Q Low when checking K_1, K_2, M_1, M_2 (Set Open)	$BV_{IN} "1"$	+5.5 1.0 0	+5.5 1.0 0	+5.5 1.0 0	Volts Min. mA Volts
Input (OFF Level) Breakdown (Clock) @ $I_{IN} =$ Other Inputs (Set Open)	$BV_{IN} "1"$	+5.5 2.0 0	+5.5 2.0 0	+5.5 2.0 0	Volts Min. mA Volts
Input (ON Level) Breakdown Voltage (All except Clock) @ $I_{IN} =$ Other Inputs: Q Low when checking Set, J_1, J_2, L_1, L_2 Set Low when checking K_1, K_2, M_1, M_2	$BV_{IN} "0"$	+5.5 1.0 Open	+5.5 1.0 Open	+5.5 1.0 Open	Volts Min. mA mA
Input (ON Level) Breakdown Voltage (for Clock) @ $I_{IN} =$ Other Inputs: $\bar{Q}$ Low when checking Clock Input at "J" Side Q High when checking Clock Input at "K" Side	$BV_{IN} "0"$	+5.5 4.0 Open	+5.5 4.0 Open	+5.5 4.0 Open	Volts mA mA
Logic "1" Threshold Voltage (for Set) $V_{OUT} =$ $I_{OUT}(SF-60)$ $I_{OUT}(SF-61)$	$V_{TH} "1"$	2.0 0.45 20 10	1.7 0.45 20 10	1.4 0.45 20 10	Volts Volts Max. mA mA
Logic "0" Threshold Voltage (for Set) $V_{OUT} =$ $I_{OUT}(SF-60)$ $I_{OUT}(SF-61)$	$V_{TH} "0"$	1.0 2.5 1.5 -0.7	1.2 2.4 1.5 -0.7	0.9 2.7 1.5 -0.7	Volts Volts Min. mA mA
OUTPUT:					
Output Leakage Current @ $V_{OUT} =$ Inputs (Set Open)	I_{OLK}	0.65 +4.5 0	0.65 +4.5 0	0.65 +4.5 0	mA Max. Volts Volts
Output Breakdown Current @ V_{OUT} Inputs	I_O	4.25 5.5 0	4.25 5.5 0	4.25 5.5 0	mA Max. Volts Volts
Output Short Circuit Current @ Input, and V_{OUT}	I_{SC}	0	45 90 0	0	mA Min. mA Max. Volts
Logic "0" Level @ $V_{IN} =$ $I_{OUT}(SF-60)$ $I_{OUT}(SF-61)$	Logic "0"	0.40 2.8 20 10	0.40 2.8 20 10	0.45 2.8 20 10	Volts Max. Volts mA mA
Logic "1" Level @ $V_{IN} =$ $I_{OUT}(SF-60)$ $I_{OUT}(SF-61)$ Opposite Output	Logic "1"	2.8 Open -1.5 -0.7 0	3.2 Open -1.5 -0.7 0	3.35 Open -1.5 -0.7 0	Volts Min. mA mA Volts
POWER REQUIREMENTS:					
"0" State Current Drain Inputs	$I_{CC} "0"$	12 Open	12 Open	12 Open	mA Max.
"1" State Current Drain Inputs	$I_{CC} "1"$	12 Open	12 Open	12 Open	mA Max. Volts

TYPICAL TEST CONFIGURATIONS

Fig. No.

1

1

1

2

2

3

3

2

2

3

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4

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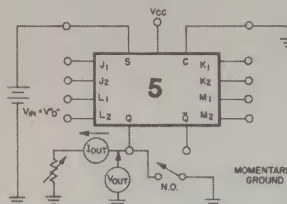
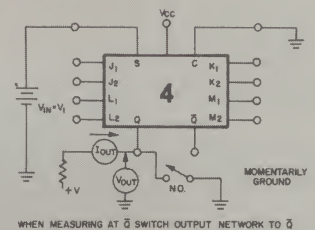
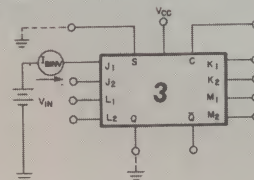
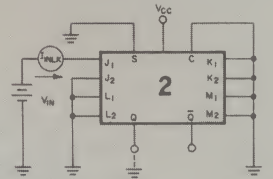
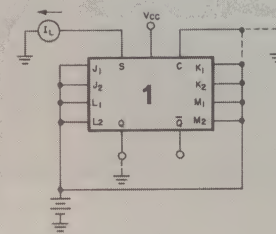
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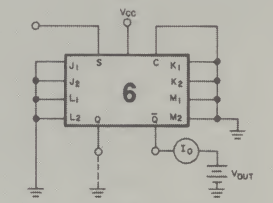
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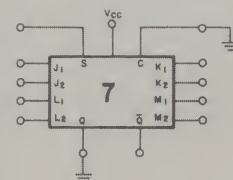
7



WHEN MEASURING AT Q SWITCH OUTPUT NETWORK TO Q



SIMILARLY FOR Q GROUND SET



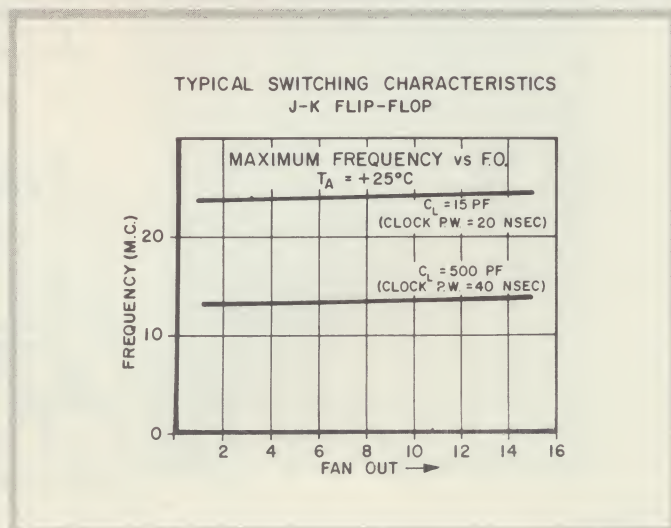
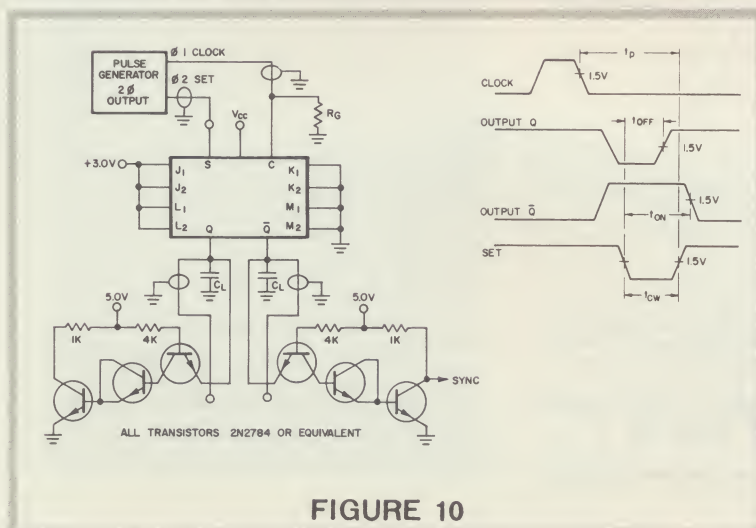
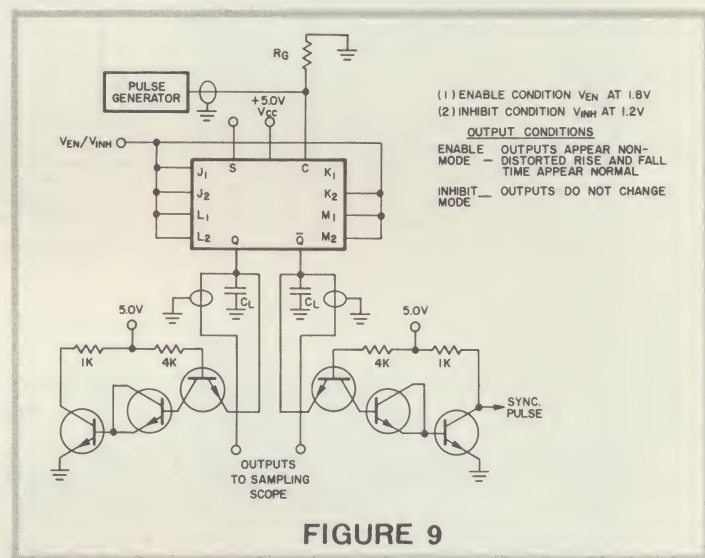
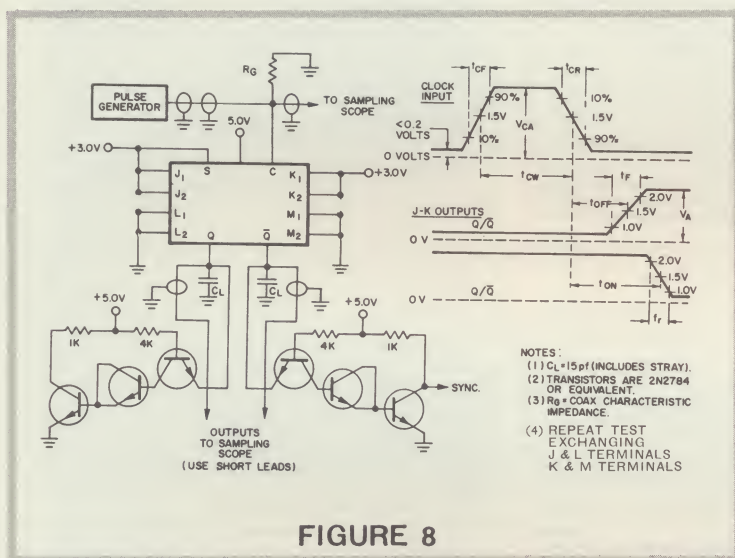
SIMILARLY FOR "1" STATE GROUND Q

J-K SWITCHING CHARACTERISTICS

FOR ALL OPERATING CONDITIONS

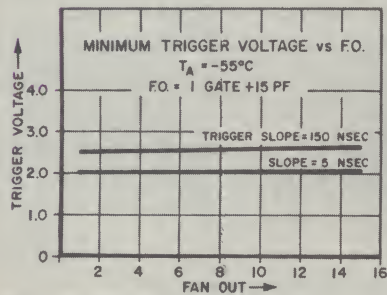
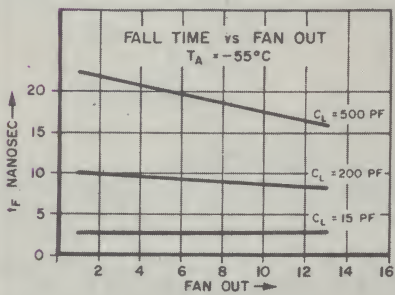
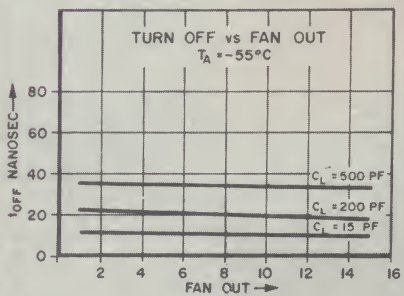
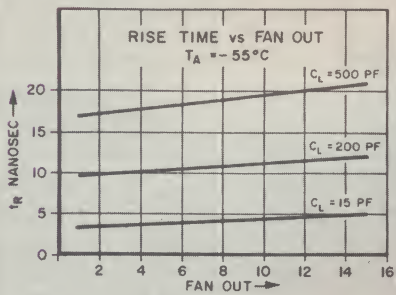
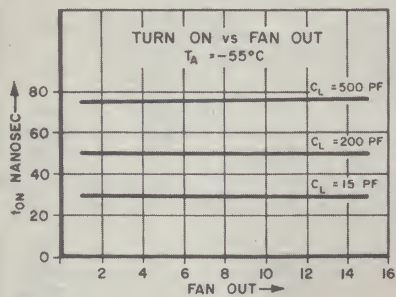
$T_A = +25^\circ\text{C}$
 $V_{CC} = 5.0\text{ V}$
 Load = F.O. = 1
 $C_L = 15\text{ PF}$

TEST	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	FIG.	
1. Output Switching Charact. (Toggle Cond.)		CLOCK					
A) Turn-Off Delay	t_{OFF}	$V_{CA} = 3.5\text{ V}$ $t_{CR} = t_{CI} \leq 10\text{ nsec}$ $t_{CW} = 100\text{ nsec}$ Freq = 5 M.C.		20	nsec	8	
B) Turn-On Delay	t_{ON}			40	nsec		
C) Rise Time	t_R			5.0	nsec		
D) Fall Time	t_F			8.0	nsec		
E) Amplitude	V_A		3.2		Volts		
2. Trigger Conditions (Toggle Cond.)							
A) Clock Pulse Width	t_{CW}	Same as in 1. Except for t_{CW}	20		nsec	8	
B) Clock Amplitude	V_{CA}	Same as in 1. Except V_{CA}	1.8		Volts		
C) Clock Slope (Neg. Going)	t_{CR}	$V_{CA} = 3.5\text{ V}$ $t_{CF} \leq 50\text{ nsec}$ $t_{CW} = 100\text{ nsec}$ Freq = 1 M.C.		200	nsec		
3. J-K Terminal							
A) Enable Level	V_{EN}	Same as in 1.	1.8		Volts	9	
B) Inhibit Level	V_{INH}			1.2	Volts		
4. Set Terminal							
A) Post Time Setting time after negative clock edge. (Flip-flop has changed state)	t_P	Same as in 1.	Set (2 ϕ Clock) $t_R = t_F = 10\text{ nsec}$ $V_{CA} = 3.5\text{ V}$ Freq = 5 M.C.	120		nsec	10
B) Pulse Width	t_{CW}		40		nsec		
C) Turn-ON Delay	t_{DON}			40	nsec		
D) Turn-OFF Delay	t_{DOFF}			20	nsec		

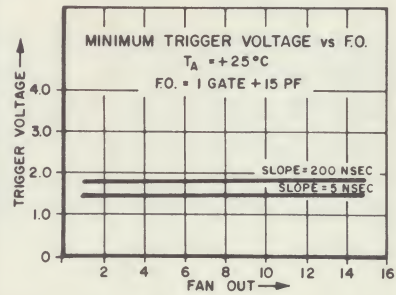
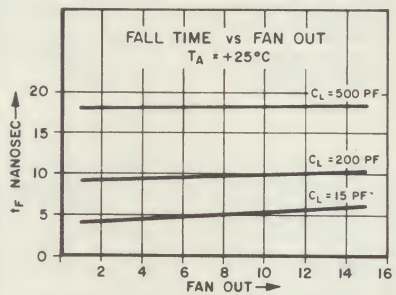
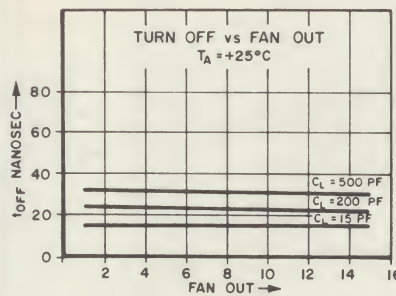
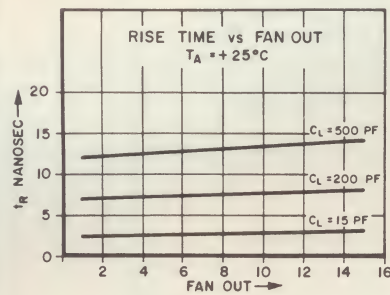
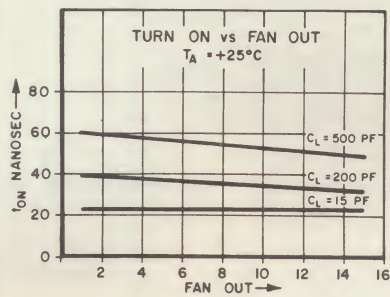


TYPICAL SWITCHING CHARACTERISTICS

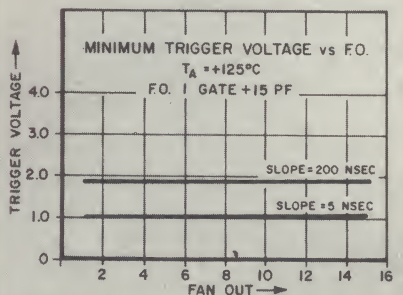
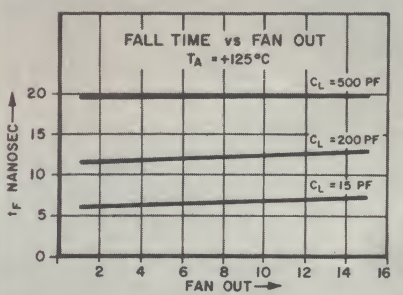
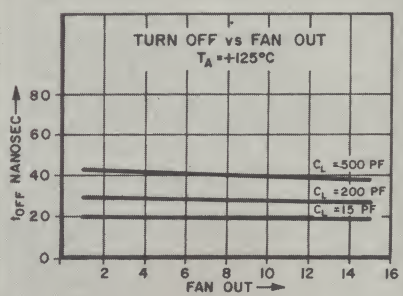
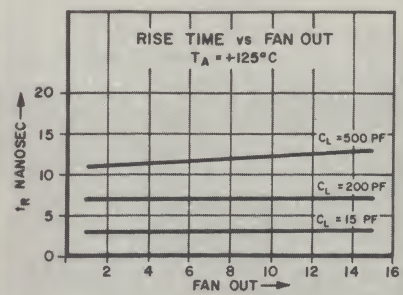
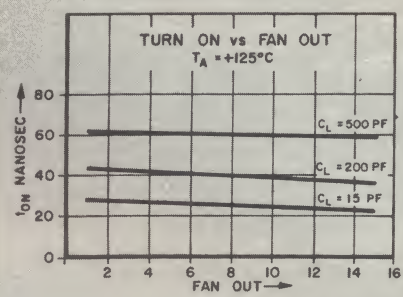
-55°C



+25°C



+125°C

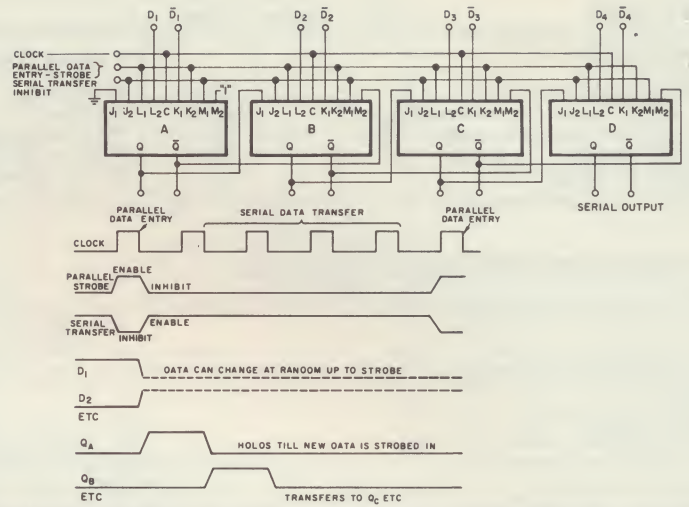


APPLICATION no. 1.

Parallel to Serial Converter

Data is inserted through one set of ORed inputs on each flip-flop when the strobe allows. The data is transferred serially through the other set of ORed inputs when the inhibit is high.

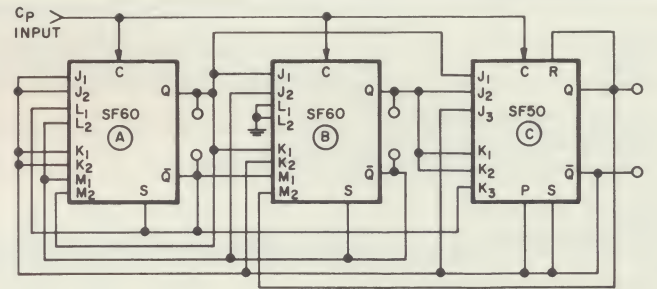
All Flip-Flops SF60 Series



APPLICATION no. 2.

20mc Synchronous Counter (Radix 7) or 20mc Frequency Divider $\div 7$

By using SUHL "OR" J-K flip-flops (SF60 series) and "AND" J-K flip-flops (SF50 series) counting and frequency dividing requirements are simplified. The set and reset inputs are shown connected to the Q and $\bar{Q}$ respectively for maximum speed, since they are not used. For putting information into the set and reset, disconnect from the outputs.



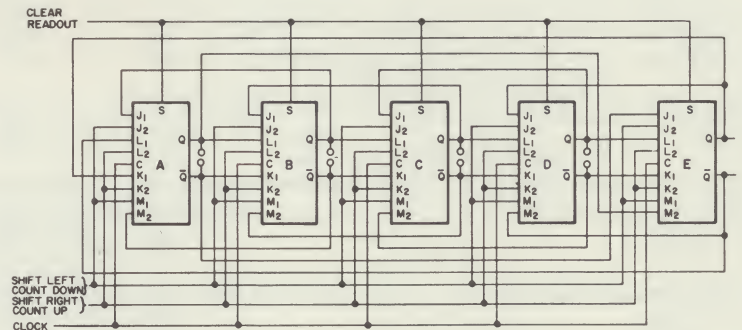
$\div 7$ OUTPUT SEQUENCE

A	B	C
0	0	0
1	0	0
2	0	1
3	1	0
4	1	1
5	0	1
6	0	0
7	0	0

APPLICATION no. 3.

Up Down Shift or Circulating Ring Counter with Read Out (Decade Shown)

Circuit shown is a high speed synchronous circulating up-down shift counter. The availability of the OR function built into the SF-60 series SUHL flip-flop allows this complex function in few packages. Gates having only two inputs are required for decoding. Decoding is done so that the counter can be cleared by use of the set input.



A	B	C	D	E
0	1	2	3	4
1	2	3	4	5
2	3	4	5	6
3	4	5	6	7
4	5	6	7	8
5	6	7	8	9
6	7	8	9	0
7	8	9	0	1
8	9	0	1	2
9	0	1	2	3

FLIP-FLOP SF-60 SERIES
GATES SG-140 SERIES

A	B	C	D	E
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
8	0	0	0	0
9	0	0	0	0

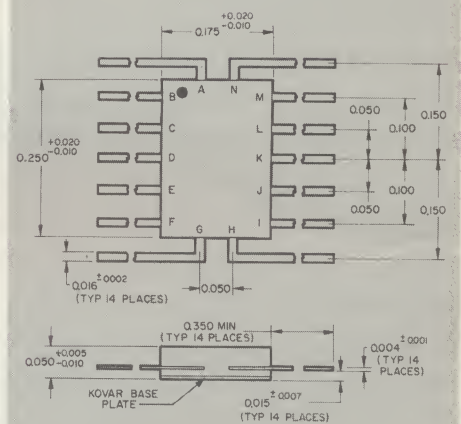
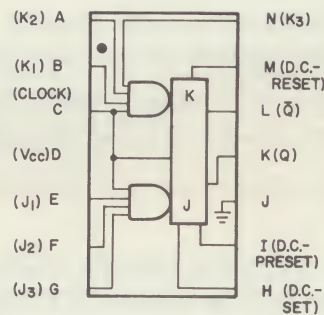
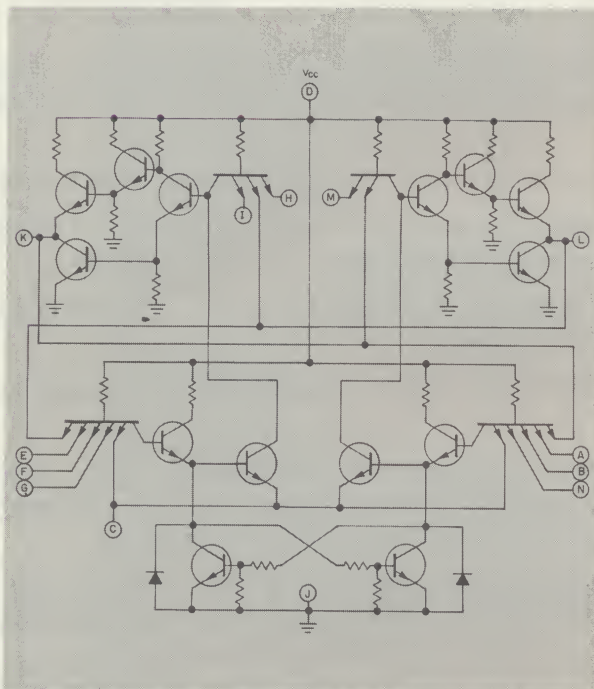
SYLVANIA
SUBSIDIARY OF
GENERAL TELEPHONE & ELECTRONICS GTE

**INTEGRATED
CIRCUITS
SUHL***

SYLVANIA

**AND Input J-K Flip-Flop
SF50/SF51**

**Monolithic Silicon Epitaxial Circuit For
Military Temp. Range -55°C to +125°C**



14 LEAD FLAT PACK—TO85
ALSO AVAILABLE IN SYLVANIA
14 LEAD PLUG-IN PACKAGE

CIRCUIT DESCRIPTION

The **SF-50** and **SF-51** are J-K flip-flop members of the SUHL* family, which is a monolithic epitaxial, saturated high speed type of logic. The circuit is designed with the system requirements in mind permitting high speed systems with a saving on gates and interconnections. The SF-50 and SF-51 operate up to 20 megacycles over the Military temperature range of -55°C to +125°C while maintaining SUHL* characteristics of fan-out, logic swing, noise immunity and capacitance drive at low power. The SUHL* J-K flip-flop operates from a single 5.0V power supply.

Information is fed into the J and/or K terminals while the clock is low. This new information is ANDed with the present state of the flip-flop (the state of the flip-flop is fed back to the input terminals via the connection from the Q and $\bar{Q}$ terminals to the K and J terminals respectively) and stored in the depletion region of a diode when the clock goes high. When the clock returns low the stored information is ANDed with the inverted clock, causing the cross coupled NAND gates to be set accordingly.

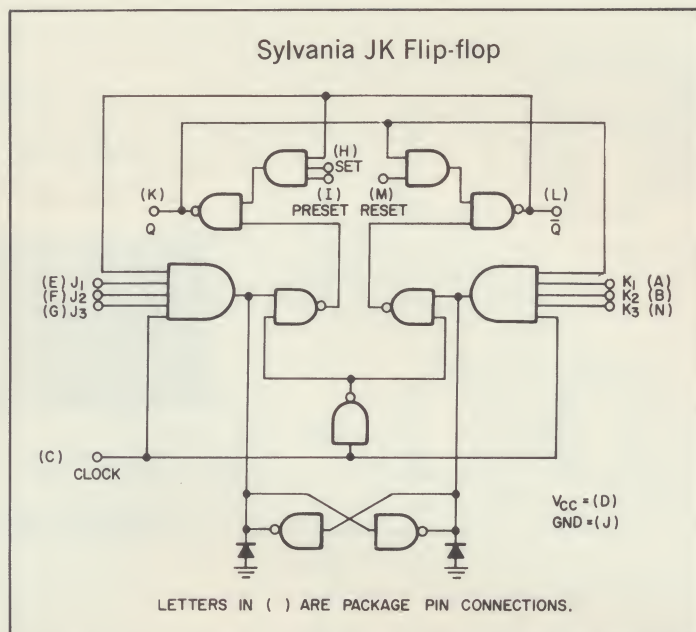
*Sylvania Universal High level Logic

Electronic Components Group / SEMICONDUCTOR DIVISION / WOBURN, MASS.

November 1, 1965

CHARACTERISTIC SUMMARY

1) Logic at the inputs—in addition to the basic J-K flip-flop function of determinate output states for every input condition, the Sylvania **SF-50** and **SF-51** have three J and three K data inputs which can be used to provide the AND function right in the flip-flop. This provides greater system speed equivalent to the speed of the flip-flop and reduces the number of external NAND gates necessary to perform system operations.**



J	K	Q _n	Q _{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

WHERE $J = J_1 \cdot J_2 \cdot J_3$
 $K = K_1 \cdot K_2 \cdot K_3$

TRUTH TABLES

$$Q_{n+1} = J \bar{Q}_n + \bar{K} Q_n$$

$$\bar{Q}_{n+1} = \bar{J} \bar{Q}_n + K Q_n$$

LOGIC EQUATIONS

- 2) Internal Complementing—The circuits are internally complemented which means all J and K terminals are usable as data inputs in all systems. This provides maximum speed and maximum fan-out from the flip-flop itself and simplifies systems wiring.
- 3) Operation at low frequencies and clock edges as long as 200 nanosecs is made possible by use of charge control devices.
- 4) Operation at frequencies greater than 20 mc is made possible by using charge control devices (instead of a master slave operation) coupled with a discharge network which removes any excess stored charge at high frequency.
- 5) Negative edge triggering—Triggering is done when the clock goes negative. This permits the rest of the system to be inhibited (positive logic) at the time the flip-flop is going through its translation.
- 6) Raceless—The inhibiting action of the clock input also directly inhibits the J and K terminals thus preventing any race problem internal to the flip-flop.
- 7) Raceless in a system where one flip-flop drives another. Data should be present when the clock goes high. If the data changes while the clock is high, the flip-flop requires 300 nsec to recognize a change from "1" to "0"; 10 nsec to recognize a change from "0" to "1". In addition, the delay through a flip-flop is greater than 8 nanoseconds.
- 8) Triggers on clock pulses as narrow as 20 nanosecs;‡ the charge storage (memory of data on J and K terminals) is accomplished rapidly through low impedances. No master flip-flop has to be set. No restriction on maximum pulse width.
- 9) Noise immune clock—Triggers on the voltage level of the clock and can therefore tolerate high noise on the clock when it is in the "1" or the "0" position. Because of this characteristic the clock input is also tolerant to overshoot up to the positive breakdown voltage and 0.5 V below ground.
- 10) Provides asynchronous (direct) SET, PRESET and RESET terminals each of which represents a gate load of 1 and is independent of the clock. The application of a "0" to H or I sets K high; to M, resets L high (or K to "0").
- 11) All J and K terminals represent a gate loading of one. The clock terminal represents a gate loading of 1.5.
- 12) High fan-out: 15 min. for **SF-50**; 7 min. for **SF-51**.
- 13) High speed: 20 mc clock. Propagation delay times typically
 13 nsec t_{off} , 25 nsec t_{on}
- 14) High noise immunity ± 900 mv at 25°C and worse case fan-out
 ± 450 mv from -55°C to +125°C and worse case fan-out.
- 15) High capacitance drive up to 600 pf.
- 16) High logic swing: Logic 0 is typically 0.26 volts, Logic 1 is typically 3.3 volts at 25°C.
- 17) Low power: typically 40 milliwatts.
- 18) Low output impedance in the "0" and "1" level reduces noise pick-up.

‡Unused emitters tied to 2.0 to 5.5 V or unused J's and K's tied to clock, unused H or I tied to L and unused M tied to K.

**See applications on back page.

RATINGS

Min. Typical Max.

Min. Typical Max.

VOLTAGE

Supply voltage (D.C.)			8.0 V _{bcc}
Supply voltage (surge, 1 sec)			12.0 V
Supply voltage (operating)	4.5	5.0	6.0 V
Input voltage			5.5 V
Output voltage			5.5 V

TEMPERATURE and POWER

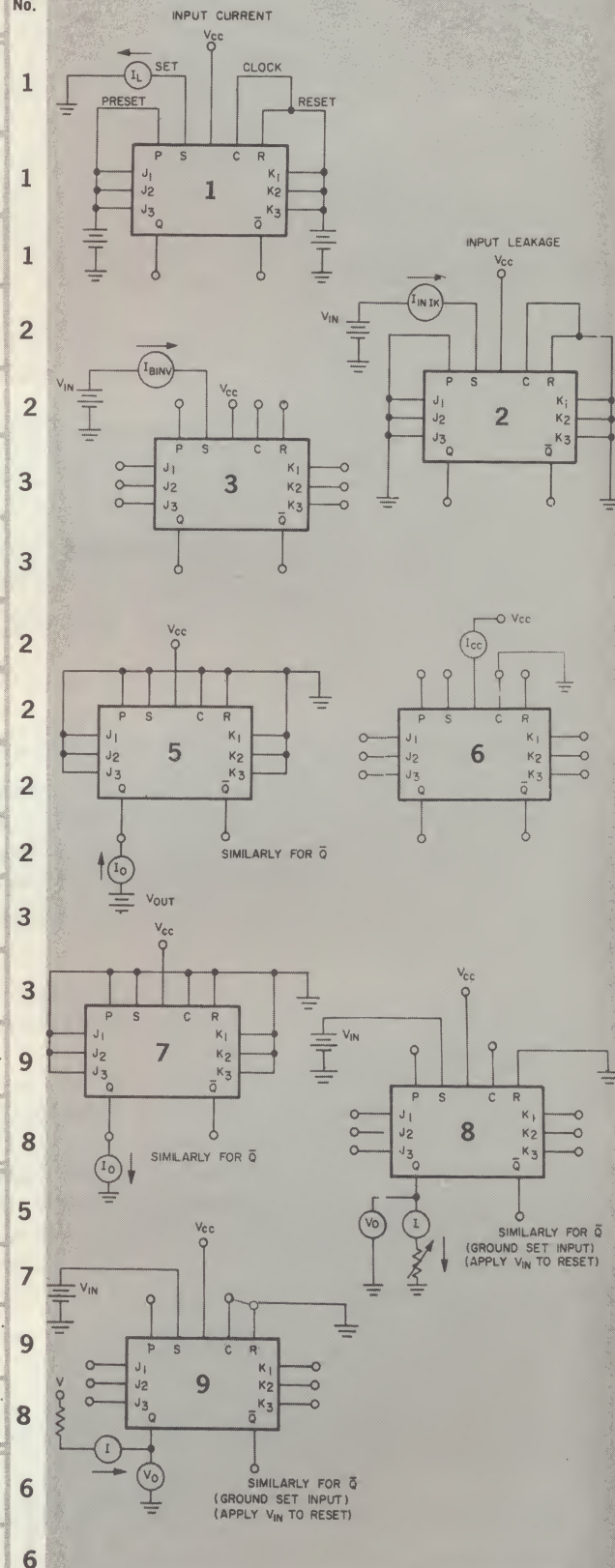
Operating	-55		+125°C
Storage	-65		+200°C
Thermal gradient, junction to air (θ_{ja})			0.3°C/MW
Thermal gradient, junction to case (θ_{jc})			0.1°C/MW
Power Dissipation (50% Duty Cycle, V _{cc} = +5v)		40	MW

ELECTRICAL CHARACTERISTICS

Characteristics at V _{CC} = +5.0V		Values at Required Temperatures			Units
Symbol		-55°C	+25°C	+125°C	
INPUT:					
Input Load Current (For set, preset, reset)	I _L	1.33	1.33	1.33	mA Max.
④ V _{IN} =		0	0	0	Volts
Other Inputs: Ground Set when checking Reset		+4.5	+4.5	+4.5	Volts
Ground Reset when checking Set, Preset					
Input Load Current (For J ₁ , J ₂ , J ₃ , K ₁ , K ₂ , K ₃)	I _L	1.33	1.33	1.33	mA Max.
④ V _{IN} =		0	0	0	Volts
Reset when checking J ₁ , J ₂ , J ₃		0	0	0	Volts
Set when checking K ₁ , K ₂ , K ₃		+4.5	+4.5	+4.5	Volts
Others					
Input Load Current (for Clock)	I _L	2.0	2.0	2.0	mA Max.
④ V _{IN} =		0	0	0	Volts
Others		+4.5	+4.5	+4.5	Volts
Input Leakage Current (All except Clock)	I _{IN LK}	0.1	0.1	0.1	mA Max.
④ V _{IN} =		+4.5	+4.5	+4.5	Volts
Other Inputs: To Test Set and Preset, Gnd. $\overline{Q}$, Reset Open		0	0	0	Volts
To Test Reset, Gnd. Q, Set and Preset Open					
Input Leakage Current (for Clock)	I _{IN LK}	0.15	0.15	0.15	mA Max.
④ V _{IN} =		+4.5	+4.5	+4.5	Volts
Other Inputs: (Set, Preset, Reset Open)		0	0	0	Volts
Inverse Beta Current (All except Clock)	B _{INV}	0.1	0.1	0.1	mA Max.
④ V _{IN} =		+4.5	+4.5	+4.5	Volts
Other Inputs: Reset Low when checking Set, Preset, J ₁ , J ₂ , J ₃		Open	Open	Open	
Set Low when checking Reset, K ₁ , K ₂ , K ₃					
Inverse Beta Current (Clock)	B _{INV}	1.5	1.5	1.5	mA Max.
④ V _{IN} =		+4.5	+4.5	+4.5	Volts
Other Inputs: Reset Low when checking Clock Input at J Side		Open	Open	Open	
Set Low checking Clock at K Side					
Input (OFF Level) Breakdown Voltage	BV _{IN "1"}	+5.5	+5.5	+5.5	Volts Min.
④ I _{IN} = (for J ₁ , J ₂ , J ₃ , K ₁ , K ₂ , K ₃)		1.0	1.0	1.0	mA
Other Inputs		0	0	0	Volts
Input (Off Level) Set, Preset, Breakdown	BV _{IN "1"}	+5.5	+5.5	+5.5	Volts Min.
④ I _{IN} =		1.0	1.0	1.0	mA
Reset Input		Open	Open	Open	
Other Inputs, Q		0	0	0	Volts
Input (Off Level) Reset, Breakdown	BV _{IN "1"}	+5.5	+5.5	+5.5	Volts Min.
④ I _{IN} =		1.0	1.0	1.0	mA
Set, Preset Input		Open	Open	Open	
Other Inputs, Q		0	0	0	Volts
Input (Off Level) Clock Breakdown	BV _{IN "1"}	+5.5	+5.5	+5.5	Volts Min.
④ I _{IN} =		2.0	2.0	2.0	mA
Other Inputs (Set, Preset, Reset Open)		0	0	0	Volts
Input (ON Level) Breakdown Voltage (All except Clock)	BV _{IN "0"}	+5.5	+5.5	+5.5	Volts Min.
④ I _{IN} =		1.0	1.0	1.0	mA
Other Inputs: Reset Low when checking Set, Preset, J ₁ , J ₂ , J ₃		Open	Open	Open	
Set Low when checking Reset, K ₁ , K ₂ , K ₃					
Input (ON Level) Breakdown Voltage (for Clock)	BV _{IN "0"}	+5.5	+5.5	+5.5	Volts Min.
④ I _{IN} =		2.0	2.0	2.0	mA
Other Inputs: Reset Low when checking Clock Input at "J" Side		Open	Open	Open	
Set Low when checking Clock Input at "K" Side					
Logic "1" Threshold Voltage (for Preset, Set, Reset)	V _{TH "1"}	2.0	1.7	1.4	Volts
V _{OUT} =		0.45	0.45	0.45	Volts Max.
I _{OUT} (SF-50)		20	20	20	mA
I _{OUT} (SF-51)		10	10	10	mA
Logic "0" Threshold Voltage (for Preset, Set, Reset)	V _{TH "0"}	1.0	1.2	0.9	Volts
V _{OUT} =		2.5	2.4	2.7	Volts Min.
I _{OUT} (SF-50)		-1.5	-1.5	-1.5	mA
I _{OUT} (SF-51)		-0.7	-0.7	-0.7	mA
OUTPUT:					
Output Leakage Current	I _{O LK}	2.25	2.25	2.25	mA Max.
④ V _{OUT} =		+5.5	+5.5	+5.5	Volts
Inputs		0	0	0	Volts
Output Short Circuit Current	I _{SC}		45		mA Min.
Input @			90		mA Max.
			0		Volts
Logic "0" Level	Logic "0"	0.4	0.4	0.45	Volts Max.
④ V _{IN} =		2.8	2.8	2.8	Volts
I _{OUT} (SF-50)		20	20	20	mA
I _{OUT} (SF-51)		10	10	10	mA
Logic "1" Level	Logic "1"	2.8	3.2	3.35	Volts Min.
④ V _{IN} =		0.45	0.45	0.45	Volts
I _{OUT} (SF-50)		-1.5	-1.5	-1.5	mA
I _{OUT} (SF-51)		-0.7	-0.7	-0.7	mA
POWER REQUIREMENTS:					
"0" State Current Drain	I _{CC "0"}	12	12	12	mA Max.
Inputs		Open	Open	Open	
Reset and Clock		0	0	0	Volts
"1" State Current Drain	I _{CC "1"}	12	12	12	mA Max.
Inputs		Open	Open	Open	
Set and Clock		0	0	0	Volts

TYPICAL TEST CONFIGURATION

Fig. No.



J-K SWITCHING CHARACTERISTICS

FOR ALL OPERATING CONDITIONS

$T_A = +25^\circ\text{C}$
 $V_{CC} = 5.0\text{V}$
 $\text{Load} = F.O. = 1$
 $C_L = 15\text{ PF}$

TEST	SYMBOL	CONDITIONS		MIN.	MAX.	UNIT.	FIG.
1. Output Switching Charact. (Toggle Cond.)			CLOCK				
A) Turn-Off Delay	t_{OFF}	$V_{CA} = 3.5\text{ V}$ $t_{CR} = t_{CF} \leq 10\text{ nsec}$ $t_{CW} = 100\text{ nsec}$ Freq = 5 M.C.		3.2	20	nsec	10
B) Turn-On Delay	t_{ON}				40	nsec	
C) Rise Time	t_R				5.0	nsec	
D) Fall Time	t_F				8.0	nsec	
E) Amplitude	V_A					Volts	
2. Trigger Conditions (Toggle Cond.)							
A) Clock Pulse Width	t_{CW}	Same as in 1. Except for t_{CW}	Output must complement with each clock pulse	20	200	nsec	10
B) Clock Amplitude	V_{CA}	Same as in 1. Except V_{CA}		1.8		Volts	
C) Clock Slope (Neg. Going)	t_{CR}	$V_{CA} = 3.5\text{ V}$ $t_{CF} \leq 50\text{ nsec}$ $t_{CW} = 100\text{ nsec}$ Freq = 1 M.C.				nsec	
3. J-K Terminal							
A) Enable Level	V_{EN}	Same as in 1.		1.8	1.2	Volts	11
B) Inhibit Level	V_{INH}					Volts	
4. Set-Preset-Reset Terminal							
A) Post Time Setting time after negative clock edge (FF has changed state)	t_P	Same as in 1.	Set-Preset or Reset $t_R = t_F = 10\text{ nsec}$ $V_{CA} = 3.5\text{ V}$ Freq = 5 M.C.	120	40	nsec	12
B) Pulse Width	t_{CW}						
C) Turn-ON Delay	t_{DON}						
D) Turn-OFF Delay	t_{DOFF}						

TEST SET-UP FOR MEASURING J-K FLIP FLOP (SF-50'S) SWITCHING PARAMETERS

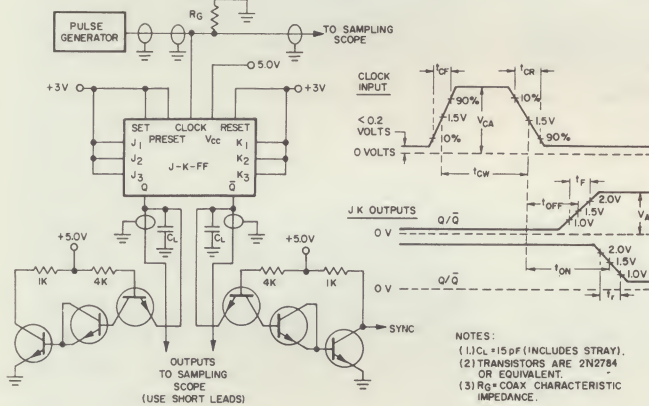


FIGURE 10

SETTING
 (1) ENABLE CONDITION V_{EN} SET AT 1.8V
 (2) INHIBIT CONDITION V_{INH} SET AT 1.2V

OUTPUT CONDITIONS
 ENABLE — OUTPUTS APPEAR NON-MODE
 DISTORTED RISE AND FALL TIME APPEAR NORMAL
 INHIBIT MODE — OUTPUTS DO NOT CHANGE

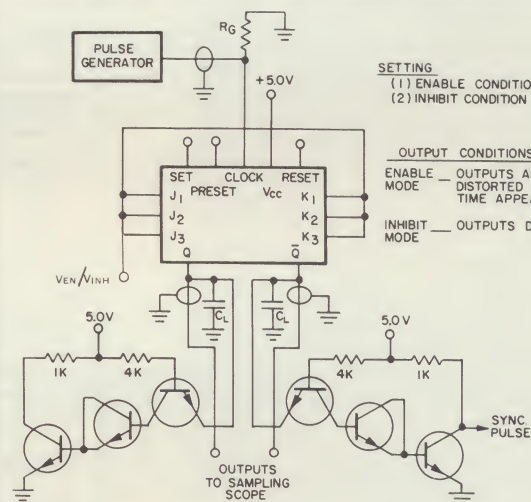


FIGURE 11

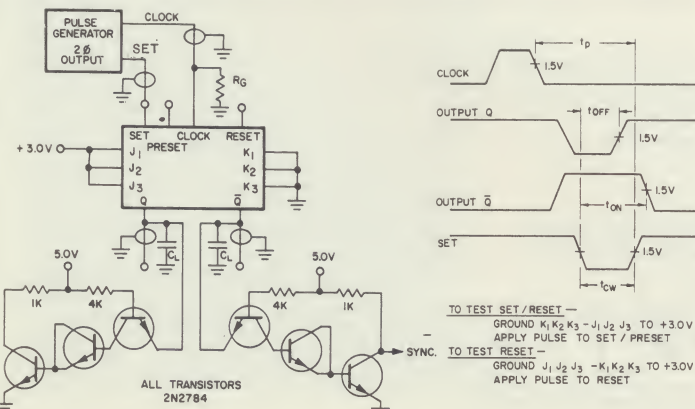
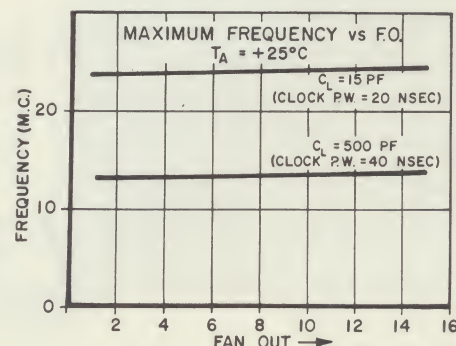


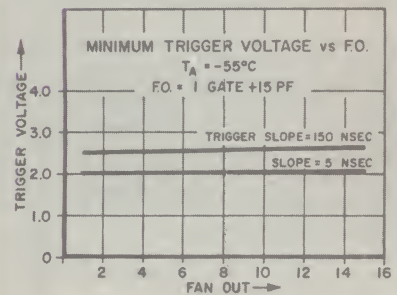
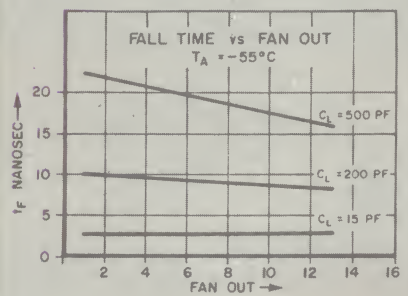
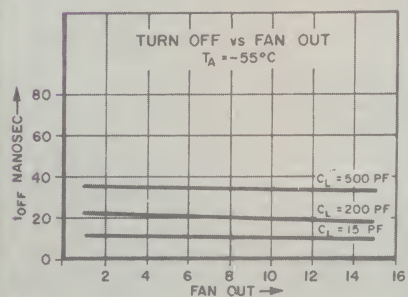
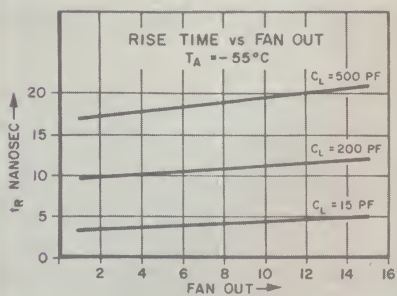
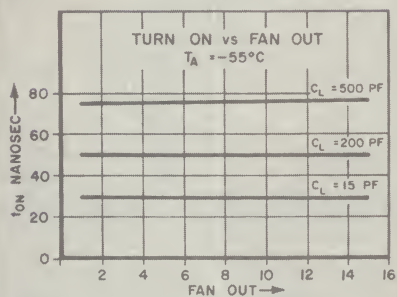
FIGURE 12

TYPICAL SWITCHING CHARACTERISTICS
 J-K FLIP-FLOP

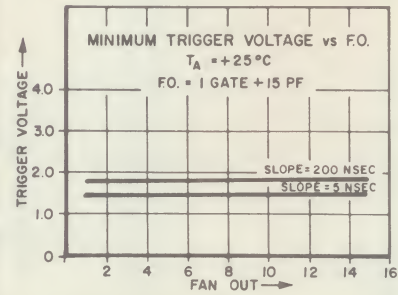
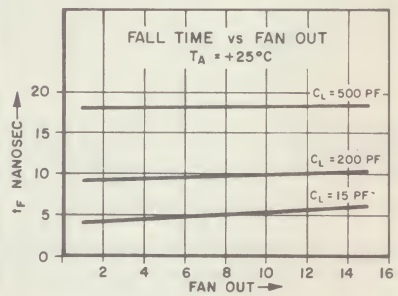
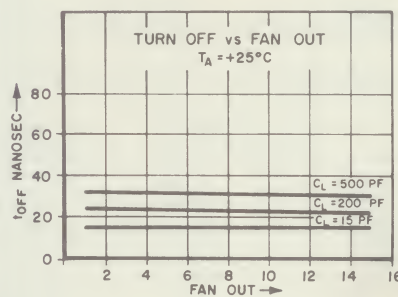
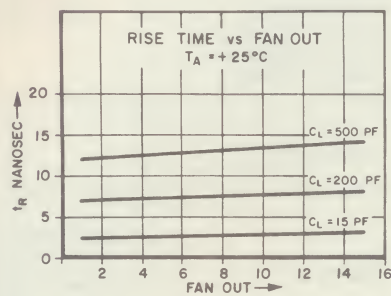
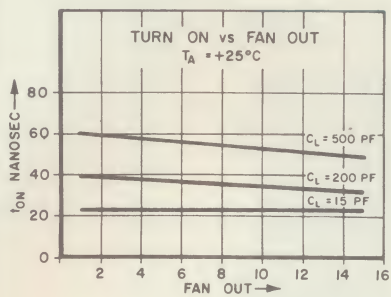


TYPICAL SWITCHING CHARACTERISTICS

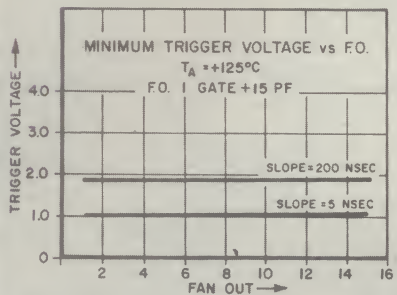
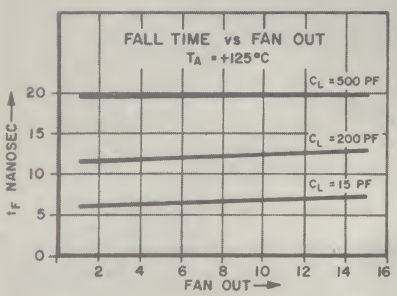
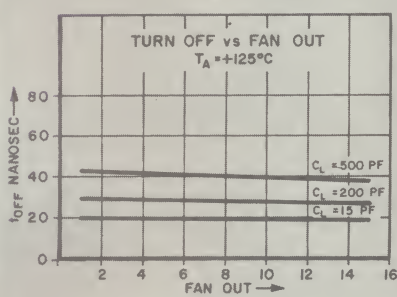
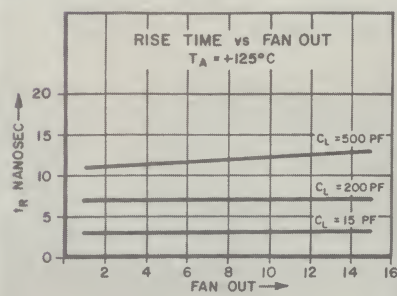
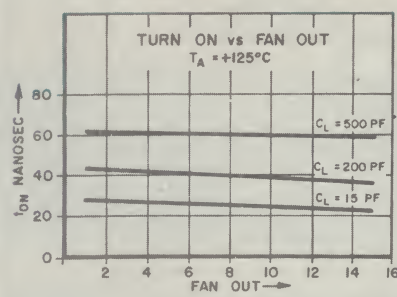
-55°C



+25°C



+125°C

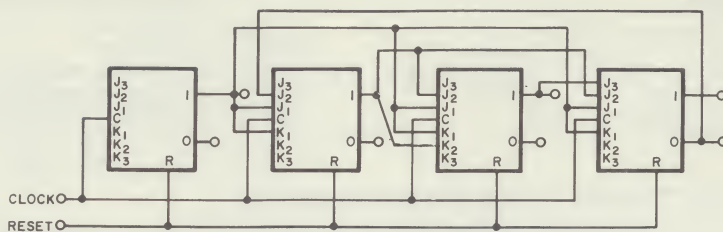


APPLICATION 1. Synchronous Binary Decade Counter

Uses only 4 Sylvania SF 50 series JK flip flops.

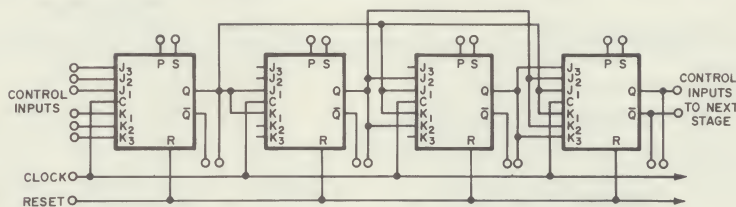
Clock frequency up to 20 mc. Counts up to 20 mc.

All outputs appear simultaneously. Output can be decoded on the next positive clock transition.



APPLICATION 2. Synchronous Binary Counter

This demonstrates the advantage of multiple J and K terminals. This uses only 4 Sylvania SF 50 series JK flip flops. Because gating is done internally this circuit has no external gate delays and can count at 20 megacycles, using 4 packages and dissipating a total of less than 200 mw.

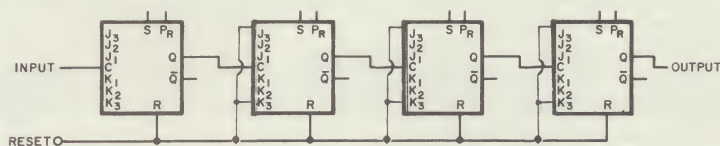


APPLICATION 3. Ripple Counter

This simple ripple counter demonstrates the simplicity of systems with Sylvania SF 50 series JK flip-flops. Counting speed = 20 mc.

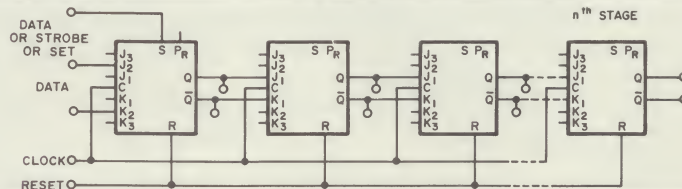
$$\text{Counting speed} = \frac{1}{n \text{ stages}} \times 30 \text{ ns/stage} = \frac{1 \times 10^9}{n \times 30} \text{ cps}$$

(For coherent outputs.)



APPLICATION 4. Serial to Parallel Converter — Shift Register

Uses 4 Sylvania SF 50 series JK Flip-flops. Clock frequency up to 20 megacycles. Shift and read out up to 20 megacycles.

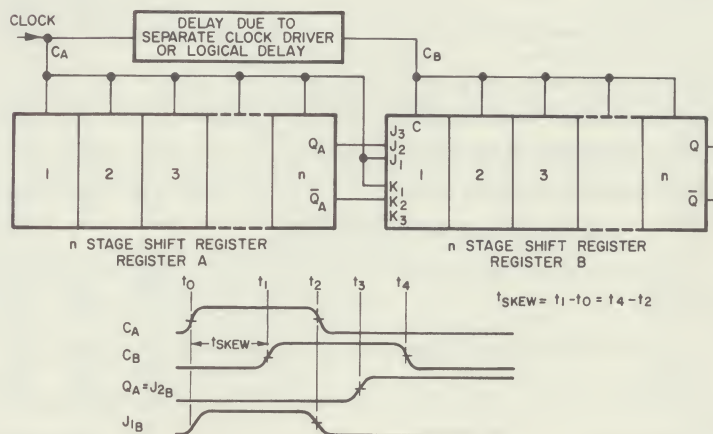


APPLICATION 5. Technique for eliminating clock skew problems

In cases where **two** registers, are driven from different clock sources because one clock driver source could not drive both registers or where a logical delay is introduced in one clock line, the output of the first register may arrive ahead of time and be recognized by the second register erroneously.

This can be solved by use of multiple J and K terminals of Sylvania SF 50 series F.F. Tie clock of Register A to J₁ and K₁ of input stage of Register B.

The input stage of Register B stores information on J_{2B} (and K_{2B}) during the time between t₁ and t₂ (must be greater than 20 nsec). At t₂, when J_{1B} (and K_{1B}) goes negative it inhibits any additional information input. Any "1" or "0" stored in stage 1 of Register B will be held for a minimum of 40 nanosecs. Clock skew can be up to 40 nanosecs.



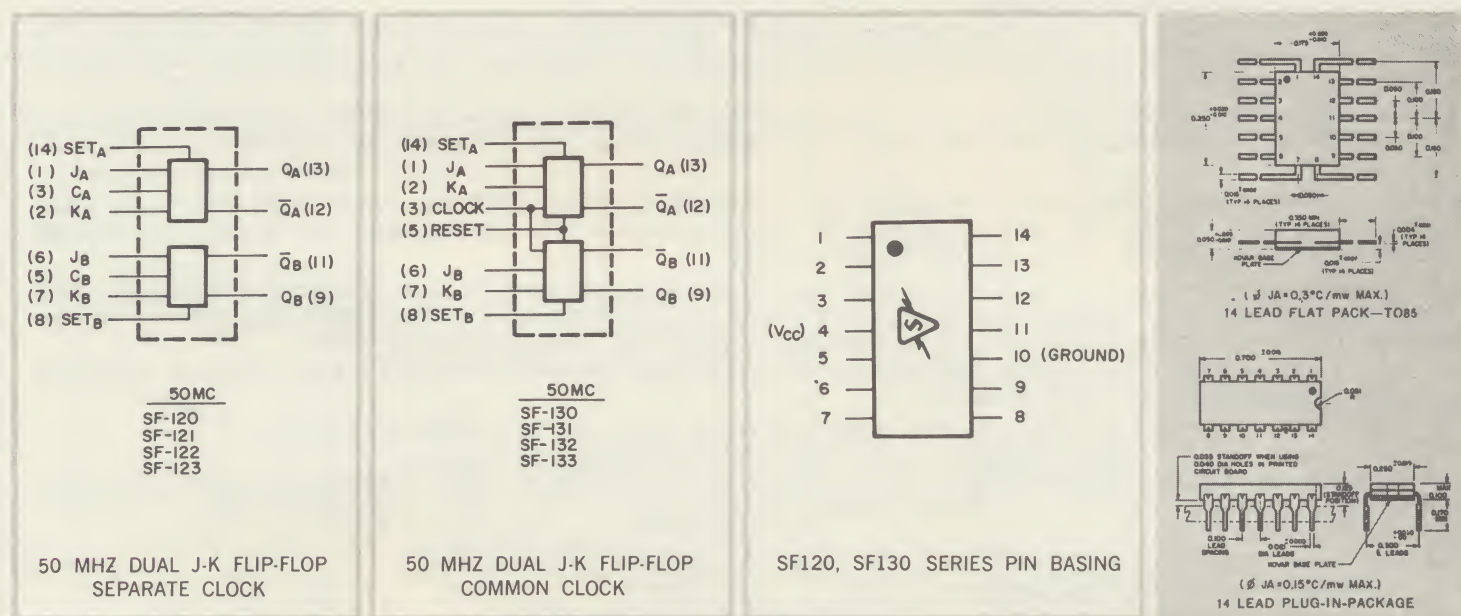
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**50 MHz Dual J-K Flip Flop
SF120 Series Separate Clock**

**50 MHz Dual J-K Flip Flop
SF130 Series Common Clock**

**NEW
PRODUCT REPORT**

Monolithic Silicon Epitaxial Circuit For Military Temp. Range -55°C to $+125^{\circ}\text{C}$ • Industrial 0°C to $+75^{\circ}\text{C}$



FUNCTIONAL DESCRIPTION

This new product report describes the **SF120**, and **SF130** series dual J-K flip-flops, which are members of the SUHL* II family of monolithic epitaxial, saturated high speed transistor-transistor logic. These dual flip-flops operate at 50 megahertz over the military temperature range of -55°C to $+125^{\circ}\text{C}$ and the industrial temperature range of 0°C to $+75^{\circ}\text{C}$, while maintaining SUHL* characteristic of fan-out, logic swing, noise immunity and capacitance drive at low power.

Information is fed into the J and/or K terminals while the clock is low. This new information is ANDed with the present state of the flip-flop (the state of the flip-flop is fed back to the input terminals via the connection from the Q and $\bar{Q}$ terminals to the K and J terminals respectively) and stored in the depletion region of a diode when the clock goes high. When the clock returns low the stored information is ANDed with the inverted clock, causing the cross coupled buffered NAND gates to be set accordingly.

Both the **SF120** and **SF130** series dual J-K flip-flops operate from a single 5.0V power supply and are available in either the 14-lead flat pack (TO85) or the 14-lead dual in-line plug in package.

The **SF120** series has separate clock input terminals for each flip-flop, whereas in the **SF130** series the clock input terminal is common to both flip-flops in the package. The **SF120** series also has a common reset terminal. However both the **SF120** and **SF130** series have separate set input terminals for each of the dual flip-flops.

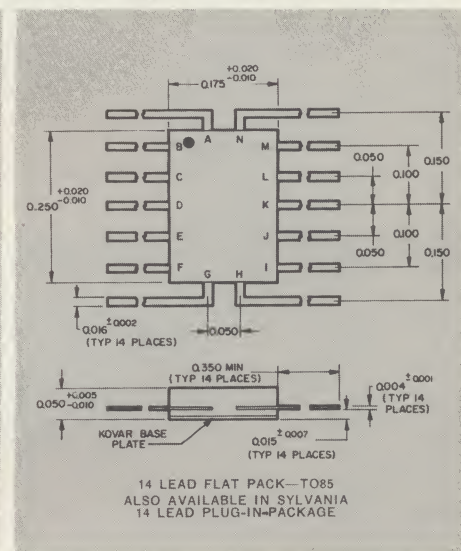
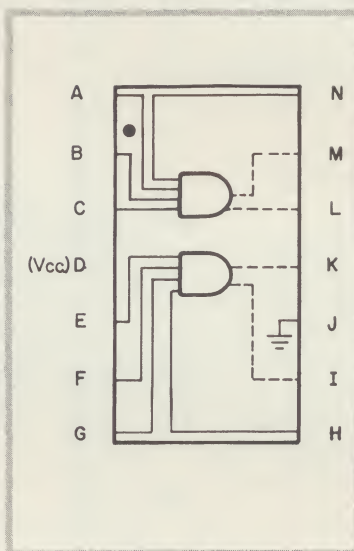
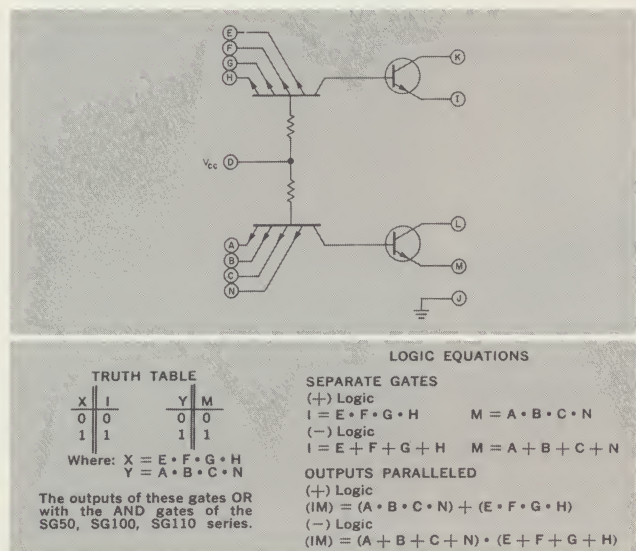
The purpose of this report is to provide tentative engineering data on Sylvania Integrated Circuits.

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INTEGRATED CIRCUITS SUHL*

Dual 4-Input OR Expander SG170/SG171

Monolithic Silicon Epitaxial Circuit For
Military Temp. Range **-55°C to +125°C**



CIRCUIT DESCRIPTION:

The **SG170** and **SG171** Dual OR expander gates, are members of the SUHL* family of logic elements, which is a monolithic, epitaxial, saturated high speed logic family. Each package contains two four-input OR expanders for use in conjunction with the SG50, SG100 or SG110 series expandable OR gates for logic applications where "OR"ing of NAND gates greater than that afforded by the basic gates is required. The capability of increasing the number of gates OR'ed makes this circuit particularly useful for adders, comparators and other "wired OR" applications. The circuit is designed for high speed operation over the full military temperature range of -55°C to $+125^{\circ}\text{C}$ without sacrificing characteristics of fan out, logic swing, noise immunity and capacitance drive at low power.

This circuit requiring only a single power supply, provides all the outstanding features of the basic SG50, SG100 or SG110 series gates to which it is added, but in addition, provides these features where "wired OR" (virtual OR) functions are required:

CHARACTERISTICS SUMMARY:

1. Low power: Add only 5 mw per gate OR'ed.
2. High fan out: Full specified fan out of gates is maintained since the ORing is done internally, not at the output.
3. High speed: Designed to operate at 20 mc. Add 1.0 nanosec to propagation delay time of basic gate for each external OR expander used.
4. Logic flexibility: By use of the **SG170** series in combination with the SG50, 100 and 110 series, AND-NOR functions having from 2 to 4 inputs/AND gate and having up to 10 AND gates OR'ed together can be obtained.
5. High Noise immunity: ± 900 mV at 25°C and worst case fan out; ± 450 mV from -55°C to $+125^{\circ}\text{C}$ at worst case fan out.
6. High capacitance drive: Up to 600 pf can be driven by gate to which it is added.
7. High logic swing: Logic 0 is typically 0.26 volts; Logic 1 is typically 3.3 volts at 25°C .
8. Short circuit protection of the basic gate.

These features offer to the logic designer for the first time in an integrated circuit the combined advantage of speed at low power, high reliability and a high degree of logic flexibility. The result is a digital element that facilitates system design when combined with other SUHL elements.

*Sylvania Universal High level Logic

Electronic Components Group / SEMICONDUCTOR DIVISION / WOBURN, MASS.

November 1, 1965

RATINGS

Min. Typical Max.

Min. Typical Max.

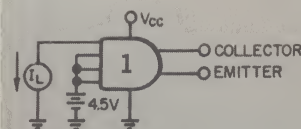
VOLTAGE			TEMPERATURE AND POWER		
Supply voltage (D.C.)		8.0 V _{DC}	Operating	-55	+125°C
Supply voltage (surge, 1 sec)		12.0 V	Storage	-65	+200°C
Supply voltage (operating)	4.5	5.0	Thermal gradient, junction to air (θ_{ja})		0.3°C/MW
Input voltage		5.5 V	Thermal gradient, junction to case (θ_{jc})		0.1°C/MW
Output voltage		5.5 V	Power Dissipation (50% Duty Cycle, V _{CC} = +5v)	5.0	MW

ELECTRICAL CHARACTERISTICS

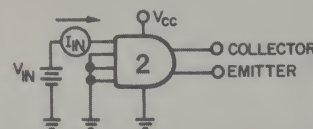
TYPICAL TEST CONFIGURATION

Characteristics at $V_{CC} = +5.0V$		Values at Required Temperatures			Units
	Symbol	$-55^{\circ}C$	$+25^{\circ}C$	$+125^{\circ}C$	
INPUT:					
Input Load Current @ $V_{IN} =$ Other Inputs	I_L	1.33 0 +4.5	1.33 0 +4.5	1.33 0 +4.5	mA Max. Volts Volts
Input Leakage Current @ $V_{IN} =$ Other Inputs	$I_{IN\ LK}$	0.1 +4.5 0	0.1 +4.5 0	0.1 +4.5 0	mA Max. Volts Volts
Inverse Beta Current @ $V_{IN} =$ Other Inputs	I_{IN}	0.1 +4.5 Open	0.1 +4.5 Open	0.1 +4.5 Open	mA Max. Volts
Input (OFF Level) Breakdown Voltage @ $I_{IN} =$ Other Inputs	$BV_{IN}\ "1"$	+5.5 1.0 0	+5.5 1.0 0	+5.5 1.0 0	Volts Min. mA Volts
Input (ON Level) Breakdown Voltage @ $I_{IN} =$ Other Inputs	$BV_{IN}\ "0"$	+5.5 1.0 Open	+5.5 1.0 Open	+5.5 1.0 Open	Volts Min. mA
Logic "1" Threshold Voltage @ $V_{ce} =$	$V_{TH}\ "1"$	2.0 0.65	1.7 0.65	1.4 0.65	Volts Typ. Volts
Logic "0" Threshold Voltage @ $V_{OUT} =$	$V_{TH}\ "0"$	1.0 4.8	1.2 4.8	0.9 4.8	Volts Typ. Volts
OUTPUT:					
Output Leakage Current @ $V_{OUT} =$ Inputs	$I_{O\ LK}$	0.25 +5.5 0	0.25 +5.5 0	0.25 +5.5 0	mA Max. Volts Volts
Logic "1" Level @ $V_{IN} =$	$V_O\ "1"$	0.65 2.8	0.65 2.8	0.65 2.8	Volts Max. Volts
Logic "0" Level @ $V_{IN} =$	$V_O\ "0"$	4.8 0.45	4.8 0.45	4.8 0.45	Volts Min. Volts
POWER REQUIREMENTS:					
Breakdown Voltage @ $I_{CC} =$ Inputs Both Sides	BV_{CC}		8.0 10 0		Volts Min. mA Volts
"ON" State Current Drain @ Inputs Both Sides	$I_{CC}\ "0"$	2.5 Open	2.5 Open	2.5 Open	mA Max.
"OFF" State Current Drain @ Inputs Both Sides	$I_{CC}\ "1"$	3.0 0	3.0 0	3.0 0	mA Max. Volts

Fig.
No.

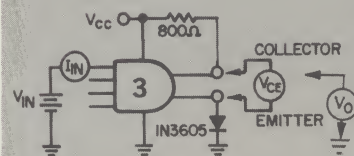


1



2

3



2

3

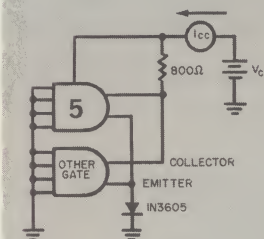
3

3

4

3

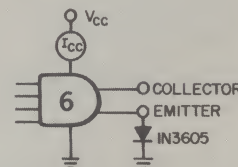
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5

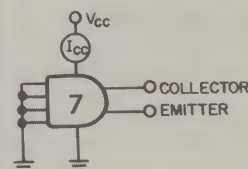
6

7



SWITCHING CHARACTERISTICS

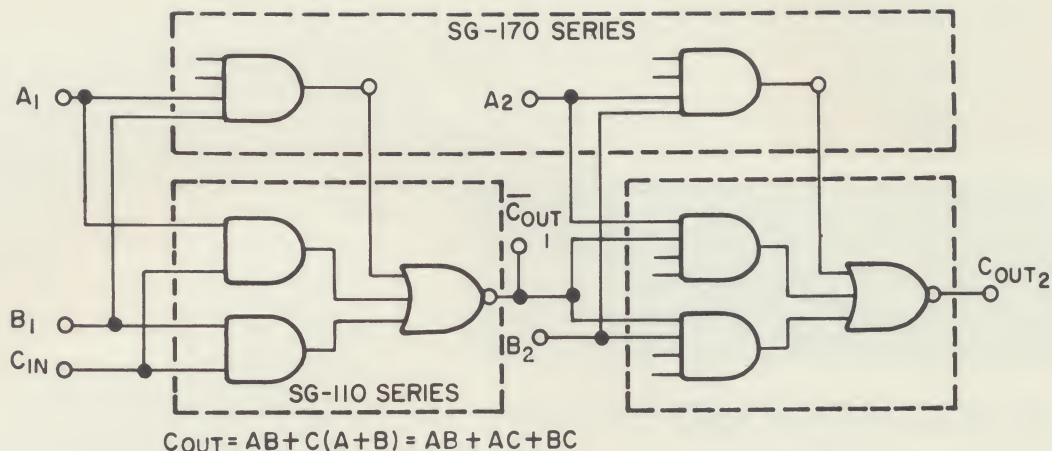
Characteristics at V _{CC} = +5.0V		Values at Required Temperatures			Units
		Symbol	−55°C	+25°C +125°C	
SWITCHING:					
Δ tpd average propagation delay effect when added to an SG50, SG100 or SG110 series gates	Δ tpd		+1.0		nsec Typ. **
Δ tpd average propagation delay due to capacitance added at expansion points	Δtpd/pf		+1.0		nsec Typ.
** With circuits removed from carrier board; short leads.					



APPLICATION 1.

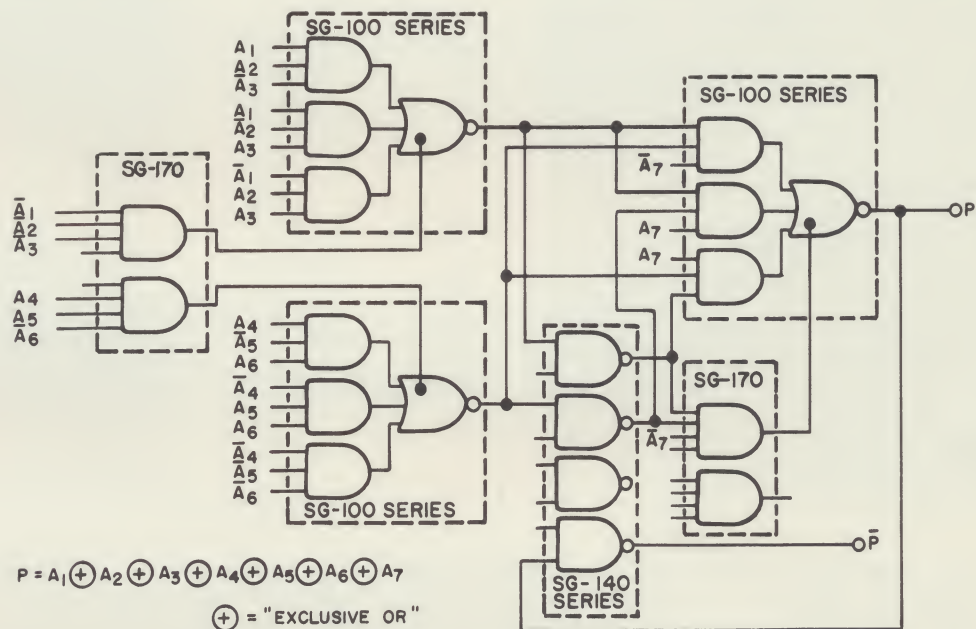
Adder Single Stage Carry

Using the OR expansion (wired OR) capability of the SG170 series.



APPLICATION 2.

Parity Generation — (7 Bits)

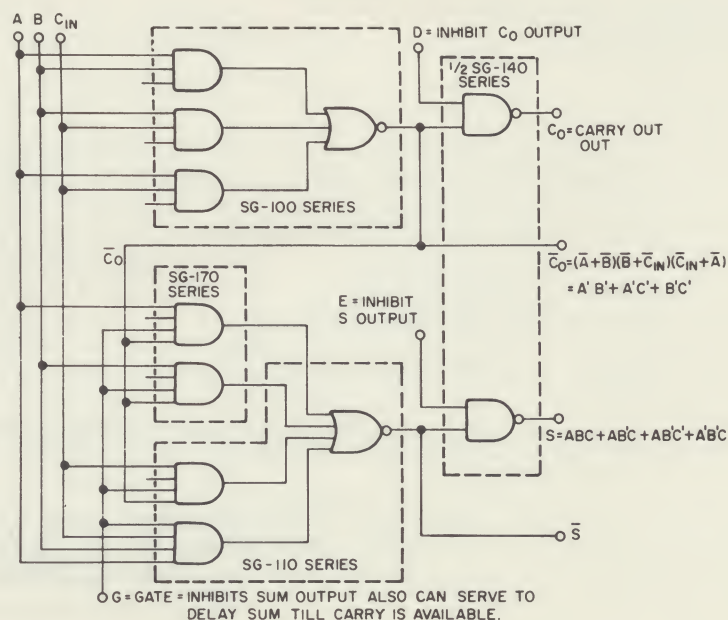


APPLICATION 3.

Full Adder

This circuit shows a Full Adder. A total of $3\frac{1}{2}$ packages are required, dissipating approximately 60 mw for the entire function. The use of the 4 inputs of the SG110 and the SG170 series as well as the expansion capability of the OR function by use of the SG170 series results in a high speed, low power, low can count system.

tpd from ABC_{in} to C_o = 15 ns
 C_o = 27 ns
 S = 15 ns plus tpd C_o
 S = 42ns



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